GROUP 19

Oil-Well Monitoring System

Senior Design I

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Sponsored by Harris Corporation

Contents

List of Tables

List of Figures

Chapter 1: Project Definition

1.1 Executive Summary

Hydrocarbons and their derivatives are a vital energy source for the world. This energy source must be managed effectively. Failure to do so often results in severe economic and environmental damage. Oil spills/leaks still remain an area of hydrocarbon management that needs improvement. The Gulf of Mexico alone is home to 27,000 abandoned oil well heads. Currently, there is no monitoring system in place to detect oil leakage from these abandoned wells. A system with the ability to actively prevent, monitor and respond to oil spills is desperately needed.

A small army of engineers has been assembled to develop such a system. A plethora of oil detection senor packages can be developed to detect underwater oil leaks. However, all of these packages require power. Obtaining useful electrical energy in the middle of the ocean is not an easy task. Nature provides three main sources of convertible energy. These include: solar, wind, and waves. A mechanical energy team has decided to design and build a hydro turbine to power a generator. Deep water ocean waves will move water over the turbine causing it to rotate. The wave generator will be placed on a large buoy that is tethered to the underwater apparatus. Several factors influence the magnitude, direction and frequency of waves. Thus, ocean waves fluctuate at random. The latter directly impacts the output of the generator. The output of the generator will be a signal of variable voltage, current and frequency. Such a signal can't be used by any electronic components. Additionally, the generator is only efficient if it operates above a particular RPM. Thus, the electrical energy from this generator must be efficiently managed, converted and stored for use by the remaining components of the system.

The team will analyze, design, build and test a low cost power management circuit. The AC signal will first be converted to high voltage DC. A step down DC-to-DC converter will bring the DC voltage down to a useable level. Also, the circuit will utilize effective control mechanisms to automatically adjust the load based on RPM input. Excess power will be stored in a battery. Power efficiency will be achieved with Maximum Power Point Tracking (MPPT). A charging circuit will be integrated into the design to allow the charging of many different types of batteries. Lastly, it will be designed to withstand harsh condition and outfitted with GPS to verify the buoy's tether remains intact.

1.1.1 Hardware Components

All of the main hardware components will be placed on one printed circuit board. The components include:

- Converters (AC-DC, DC-DC)
- Controllers
- Power Supply
- Charging Circuit
- GPS

The PCB board will be housed inside a weatherproof enclosure.

1.1.2 Software Components

The software components can be split into two main sections. PC Software will be used to interact with and reprogram the digital controllers. The controller itself will also run software that will perform some basic arithmetic.

1.2 Motivation

Energy management solutions have gained significant ground in recent years. With the push for going green, obtaining maximum energy efficiency is in high demand. The electrical engineering group would like to contribute valuable research into advanced power electronics. Hopefully the design has a significant positive impact on the clean-energy movement. The group also looks forward to representing the United States, the University of Central Florida, and Harris Engineering Corporation.

1.3 Goals

Harris Engineering Corporation will be using this system as part of their oil detection monitoring system. Therefore, success will be determined by meeting the following goals outlined below:

1. Maximize the energy supplied from the wave generator.
2. Charge several different types of batteries.
3. Protect against battery overcharging.
4. Operate over a range of 60 to 240 rpm.
5. Operate when the generator output voltage is less than the battery voltage.
6. Outfitted with GPS
7. Allow operator to monitor and control the system.

Completing these 7 steps in a timely manner is critical. The Gantt chart in Figure 1.1 will be closely followed.

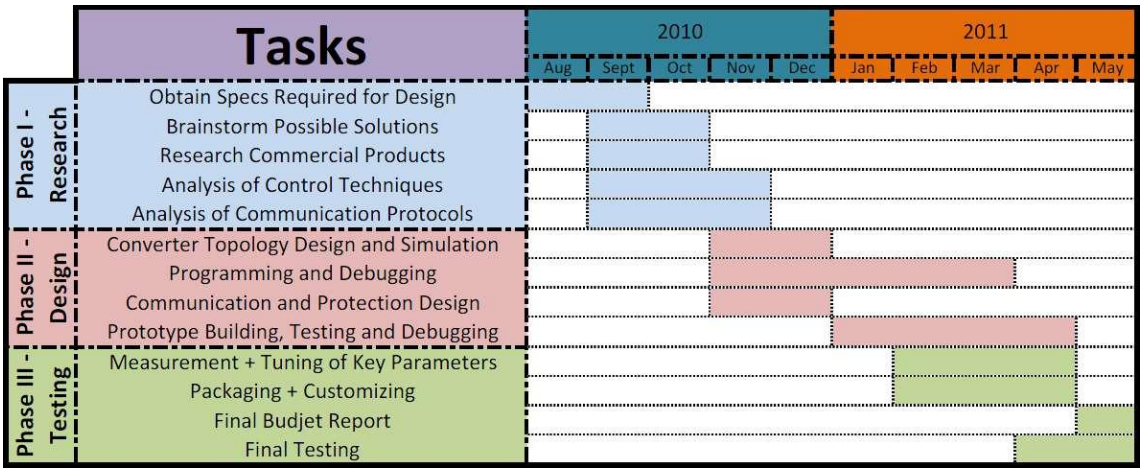


Figure 1.1 - Gantt Chart for Projected Project Completion, Electrical Team

1.4 Objectives

1.4.1 Hardware

The hardware objectives start with specifying the inputs and outputs of the system. The wave generator's output will be used as the input to the system. The system's output will be connected to a battery and sensor package. The system's goal is to transfer the power from the input to the output in the most efficient manner possible. Efficiency will be verified by connecting the system to a computer. All of the electronic components will be fitted onto a single PCB. The objectives above will be accomplished while maintaining a low parts cost.

1.4.2 Software

The software objectives are limited to PC software and controller software. The PC software will be used to program and monitor the system. Having a PC interface simplifies the development process while providing excellent logging capabilities. The onboard controller software will run a simple algorithm to help pinpoint what changes need to be made during the conversion to maintain maximum efficiency.

1.5 Requirements and Specifications

1.5.1 General Specifications

Harris Corporation has assigned four groups: three mechanical engineering groups and one electrical engineering group to be a part of this project. The mechanical engineering groups together will be in charge of development of

turbine, buoy and the sensor package. The electrical engineering group has been assigned to make sure that the necessary power is supplied to the system.

The hardware must meet the requirements as stated by Harris Corporation. According to these requirements, the system must meet the following:

- Efficiently convert a varying AC signal to a conditioned DC voltage.
- Develop an energy storage method which can continuously deliver power to the sensors.
- Design an automated generator load control system which can optimize the load control for varying input forces and generator RPM's.
- Create a GPS system which can determine and relay the buoy position for a given time.
- Create a wireless transmitter to broadcast the results of the underwater sensors.
- Must be able to work in high and low pressure environment.
- Suitable for dry and under water environment.

1.5.2 Hardware

Ginlong Generator Specifications — A Ginlong generator (Model #GL-PMG-500A) is ready to be used to develop wave energy. The electrical specifications of this generator are shown in Table 1.1

Electrical Specifications	
Rated Output Power(W)	500
Rated Rotation Speed (RPM)	450
Rectified DC Current at Rated Output (A)	20
Required Torque at Rated Power	14.8
Phase Resistance (Ohm)	5
Output Wire Square Section (mm^2)	4
Output Wire Length (mm)	600
Insulation	H Class
Generator configuration	3 Phase star connected AC output
Design Lifetime	>20 years

Table 1.1 - Eletrical Specifications of Ginlong Generator
(Permissions requested from Ginlong Technologies, Inc.)

Because the generator will be turned by wave energy harnessed through a uniquely designed turbine system, it is expected that the rotations per minute of the generator will vary significantly. No load will be placed upon the generator at startup, but the load control circuitry will ultimately be responsible for maintaining the steadiest possible rotation in the generator. Figure 1.2 shows the power (W) and voltage (V) outputs for the Ginlong generator as functions of rotation speed

(RPM). The power output is very low and grows very slowly for low rotation speeds, but at higher rotation speeds, the power output begins to climb more rapidly. The voltage output has an approximately linear relationship with rotation speed, where the voltage in volts is equal to one tenth of the rotation speed in RPM.

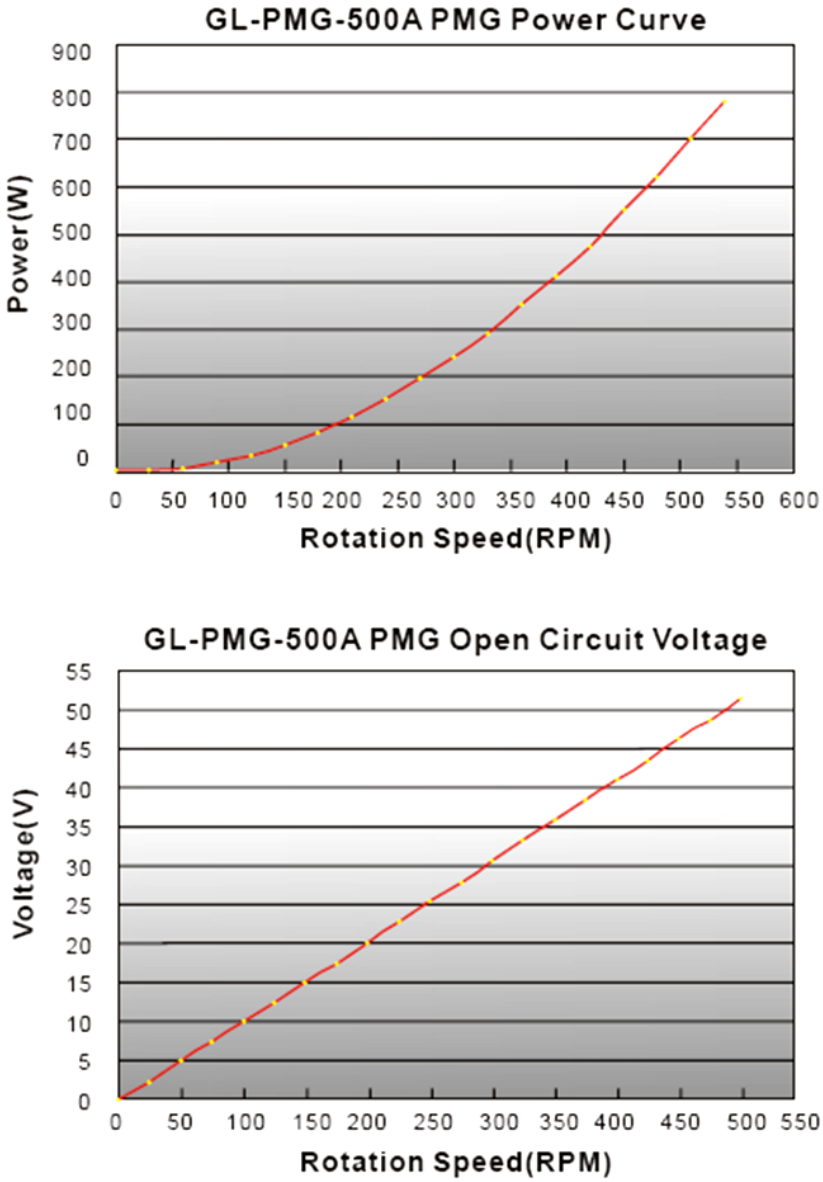


Figure 1.2 - Power v. Rotation Speed and Voltage v. Rotation Speed for the Ginlong generator (Permission requested from Ginlong Technologies, Inc.)

Sensor Power Requirements — Sensor power requirements need to be met in an efficient manner. The sensor package will be the most critical part of the project since this package will be responsible for detecting the presence of oil in

water. The sensor team will be using a Wi-Ranger to power the components (sensors, DAQ, etc.). In order to provide an efficient power supply, the Wi-Ranger specs need to be taken under consideration. According to the datasheet, the Wi-Ranger requires an external power supply with 5V DC and 3A which is 15W.

Control System — The Control System will be comprised of:

- AC-DC Rectifier
- DC-DC Buck Convertor
- PWM controller
- Analog to Digital Convertor

An **AC-DC Rectifier** will be needed to rectify the input AC signal to output DC signal. Here are the various requirements for the rectifier:

- Three phase input
- Must be able to control a sinusoidal input current
- Maintain input current to be in phase with input voltage
- Variable frequency, voltage and current
- Produce a constant DC-bus
- Generate PWM signals

A **DC-DC Converter** must regulate the input DC signal coming from the rectifier to a constant DC output signal. A major problem in creating such a converter would be its fluctuating output due to the varying nature of the wave speed. Hence, the converter will need to meet or exceed the following expectations:

- Large input voltage capability, up to 100V
- Must be able to produce a constant output voltage of 5V DC and constant output current of 3A
- Maintain low voltage ripple
- Implement error compensation loop
- Must maintain high efficiency levels

GPS Requirements — A GPS system needs to be developed in order to track the buoy. There are a few options to go about developing this system. However, the most efficient option was the one with following requirements:

- Sends one heartbeat signal per day.
- Sends an alarm when the buoy is positioned out of its desired radius.
- Returns to sleep mode when not in use.
- Is compact and easy to install
- Operates on low power.

Circuit Charging Design – An efficient circuit charging design needs to be implemented that can meet or exceed the following requirements:

- Maximize long term charging capacity
- Provide accuracy
- Be able to communicate in various conditions
- Maintain high level efficiency
- Be cost-efficient

1.5.3 Software

Generator — A software system is being used in order to simulate and test the generator results.

Load Control — Simulation tools needs to be developed that will test the system on the following concepts:

- Stability
- Voltage Regulation
- Frequency Regulation
- Power Quality
- Load Leveling

Digital Controller – A digital controller must be placed in order to compensate for error in the power systems. Here are the requirements:

- Compensate for steady-state and overshooting errors
- Maintain flexibility for rapidly changing outputs
- Easily tuned in order to achieve desirable results
- Must be able to collect data, produce various models and provide efficient tuning capabilities

GPS System — In order to track the buoy in an efficient manner, tracking software is needed that can fulfill or following requirements:

- User-friendly interface
- Able to produce heart-beat message
- Low power usage

1.5.4 System Protection

Since this system will be placed in volatile conditions, necessary steps need to be taken to ensure maximum safety. Hence, utmost care will be taken while choosing components for the design as they need to withstand various parameters such as high voltage, power, pressure, etc. If a situation may arise

such that certain components could past the threshold of the parameters mentioned above, it is highly likely to cause permanent damage to the system.

In order to protect the system from such drastic conditions, precautions will be taken. Protection will be implemented in two levels – hardware and software. Also, external protection such as epoxy resin could be used for potting transformers and inductors in order to prevent a short circuit and to maintain a stable, long-lasting life.

1.6 Budget and Financing

Due to the nature of the project, the primary costs will be for the components and testing materials. A research lab and certain other facilities will already be available for use. These facilities include PCB maker machine, test rig, hydraulic wave generator simulator, etc. Additionally, a lot of component manufacturers tend to provide discounted or free samples. Figure 1.3 provides an example of a development kit that the team plans on purchasing since the total package of the kit costs less than the individual components.

Figure 1.3 - Development Kit
(Permission requested from Mikroelektronics)

The total cost for the electrical team is expected to be less than $2,000, which will be covered by Harris Corporation.

Chapter 2: Research

2.1 Previous Works and Similar Works

One of the major hurdles in the research for this project stemmed from the fact that the various aspects of the project were split between several groups. It is necessary to research a variety of power related topics – ranging from AC-DC rectification to DC-DC step down conversion to load control – without having immediate access to information from the other groups. Not knowing definitively the specifications of the power produced by the wave generator, or the power requirements of the sensor package, research had to be conducted on a broader range.

In order to facilitate the research, it was determined practical to investigate similar previous works. While the concept of wave-generated power has existed since the 1870's [1], investigations into wave power were drastically reduced in the 1980's in favor of wind power [2]. As a result, there is a significantly greater quantity of more thorough, readily available information regarding wind power than there is for wave power. In light of the design of the wave power generator and anticipated variation in its power generation resulting from the randomness of waves, it is decided reasonable to make a comparison between the wave power provided by this project and the power provided by modern wind power generators. To this end, various aspects of power management in wind power generators were researched, including but not limited to AC-DC conversion, DC-DC step-down conversion, MOSFETs, and op-amps.

2.2 Hardware Research

2.2.1 AC-DC Rectification

The output from the wave generator is known to be AC electric power of variable magnitude. In order to power the sensor package, this needed to be converted to stable DC electric power. To accomplish this, the first aspect that is researched is AC-DC rectification.

Full Wave Bridge Rectification — A simple rectifying circuit is the full wave bridge rectifier, so named for its diode bridge. When the input voltage is positive, two of the diodes are forward biased, while the opposite two are reverse biased, providing a positive output voltage across the resistor. When the input voltage is negative, the diode biases are switched, and a positive output voltage is still produced across the resistor.

While the voltage output for the full wave bridge rectifier is a positive DC voltage, it strongly mirrors the amplitude of the input AC voltage, which is undesirable. It

is also possible to utilize a transformer to reduce the input voltage before it reaches the diode bridge, but an anticipated low maximum power supplied by the wave generator make the necessity for this reduction unlikely.

Three-Phase Full Wave Rectification — A three-phase full wave rectifying circuit, shown in Figure 2.1, is able to provide a more DC output that is closer to a constant value for a three-phase AC input. This is a result of the fact that the phase difference between the three AC waveforms, when fully rectified, is smaller than the wavelength of any one waveform.

The advantage of this circuit is a significant decrease in the DC voltage's dependency on the amplitude of the AC waveform. This would result in a reduced necessity of ripple attenuation for the DC output. However, the three-phase full wave rectifier requires more components than a full wave bridge rectifier. This would make it more expensive and require more space. It also requires a three-phase AC input.

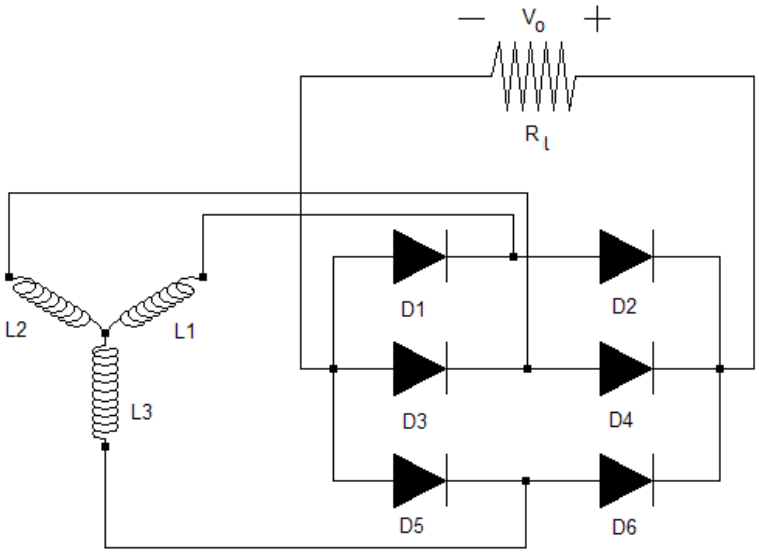


Figure 2.1 - Three-Phase Full Wave Rectifier Circuit

VIENNA Rectifier — The VIENNA rectifier is a three-phase, three-level, pulse-width modulation full wave rectifying circuit invented by Johann Kolar [3]. The circuit is shown in Figure 2.2.

The VIENNA rectifier is an extension of the full wave bridge rectifier with a boost converter for a higher DC output. It has a unity power factor [5]. Other potential advantages to the VIENNA rectifier are high power density and low switching losses. The pulse width modulation would also serve to compensate for the variable frequency power produced by the wave generator.

The VIENNA rectifier has been shown to demonstrate a wide variety of features that make it an excellent choice for this project. One of the requirements for any

rectifying circuit utilized is compatibility with the three-phase Ginlong generator. A power factor as close to one as possible is also desired. The rectifier also needs to be able to handle effectively variable amplitude, variable frequency AC voltage input because of the sporadic nature of the waves turning the generator. The VIENNA rectifier is a natural choice in light of its three-phase input, its high power factor, and its ability to rectify a voltage input with variable amplitude and frequency.

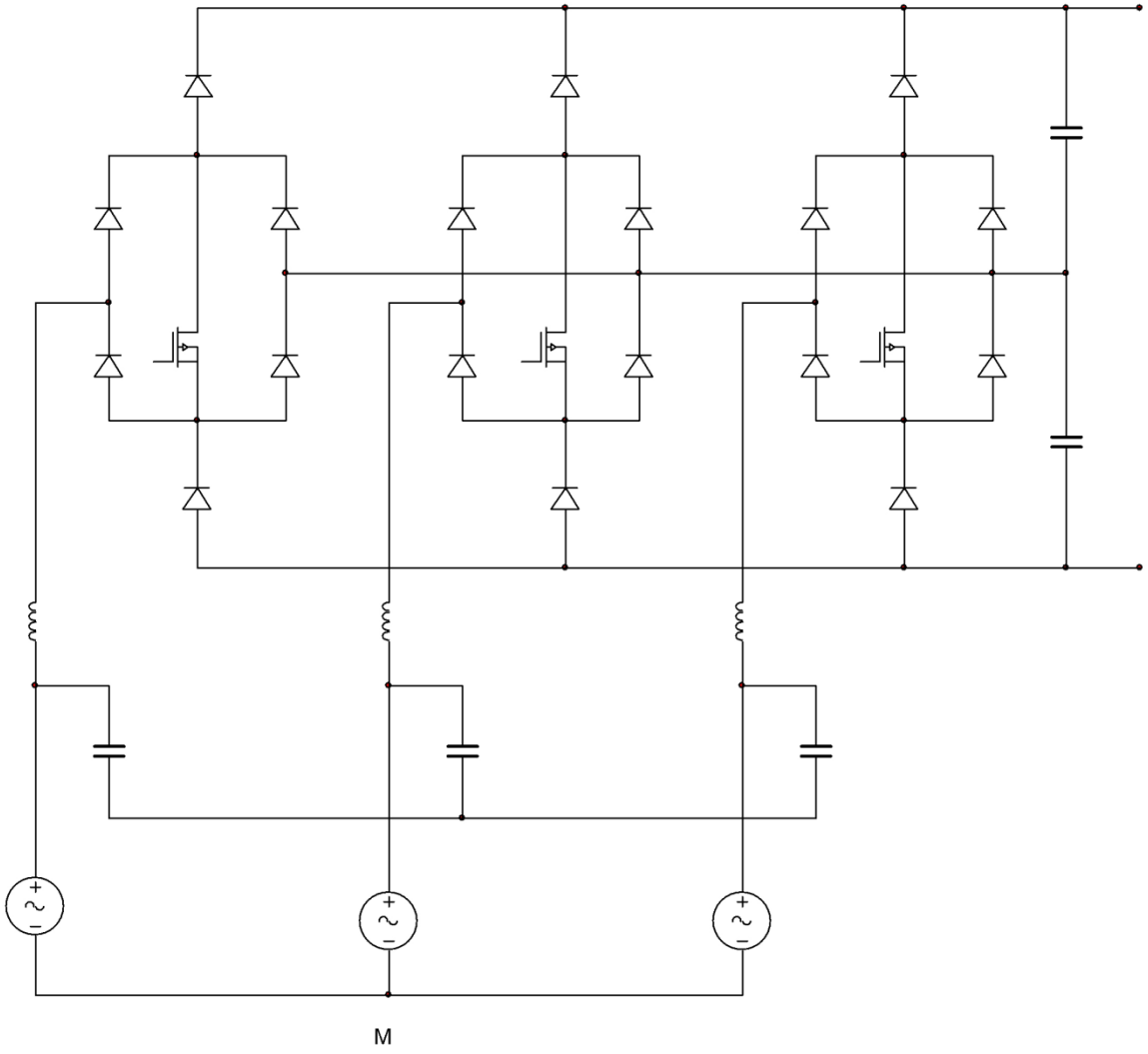


Figure 2.2 - VIENNA Rectifying Circuit

The most significant disadvantage of the VIENNA rectifier is that it functions as a two-switch boost rectifier, resulting in a significantly increased output voltage, the value of which depends on the boost ratio. The boost ratio can vary, but it is expected to be approximately 6.4 the input voltage. For a 25V input from the Ginlong generator, this would result in a voltage output from the VIENNA rectifier of 160V. DC-DC step down conversion would be required to compensate for this effect.

There are two methods of controlling the VIENNA rectifier: the hysteresis control method and the constant frequency method. A graphical depiction of the hysteresis method of control is presented in Figure 2.3. For this method, upper and lower boundaries for inductor current are set. The current is controlled through a switch to maintain a value between the established boundaries. This method has the disadvantage of complexity, but the advantage of its power harmonics being spread over a large range of frequencies.

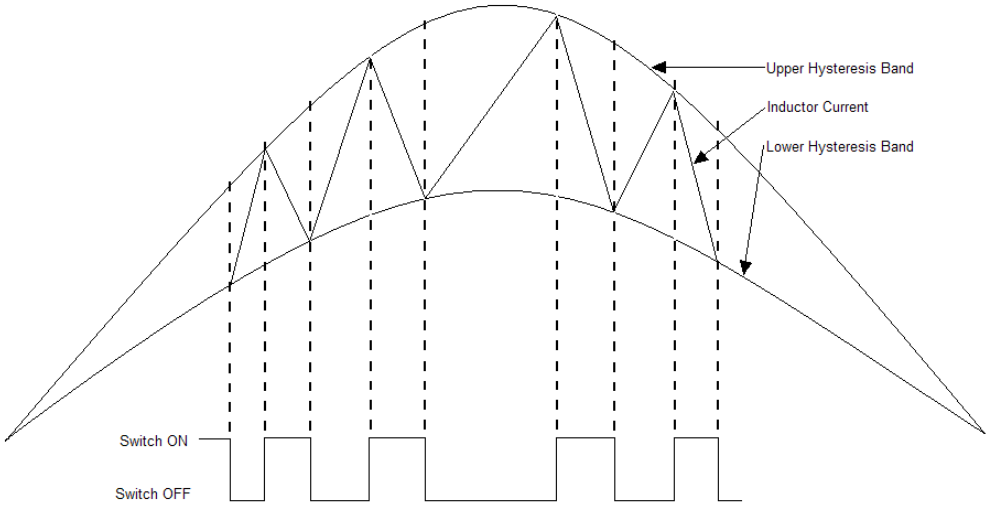


Figure 2.3 - Hysteresis Control Method for the VIENNA Rectifier

A graphical depiction of the constant frequency control method is presented in Figure 2.4. For this method of control, the control switch is switched at a constant frequency with varying pulse width.

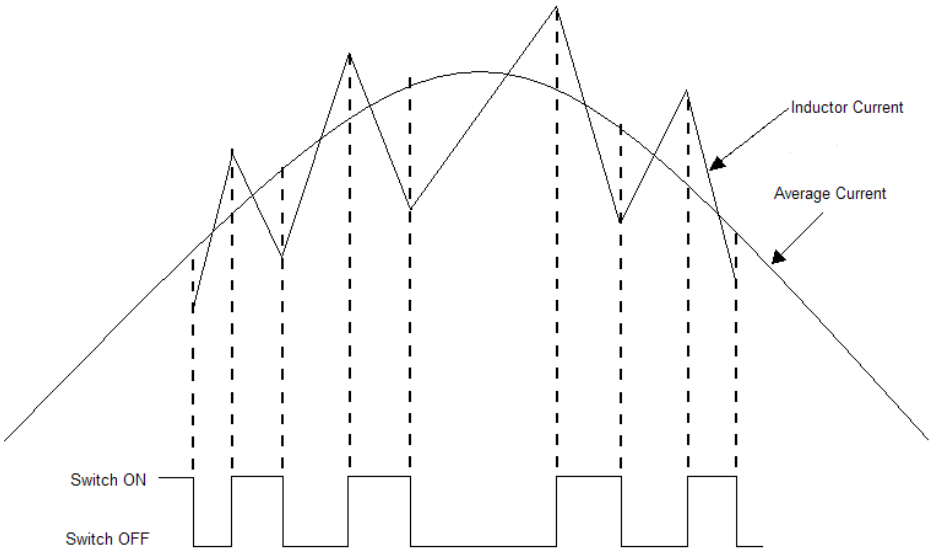


Figure 2.4 - Constant Frequency Control Method for the VIENNA Rectifier

Each of these methods has specific advantages and disadvantages that ought to be considered when deciding how best to control the VIENNA rectifier. Table 2.1 considered the comparative advantages and disadvantages to these two methods.

	Control Method	
	Constant Frequency Control	**Hysteresis Control**
Advantages	Easier EMI filtering	EMI distributed over wide spectrum
	Simple control implementation	Inherent current protection
	Single control loop for output voltage and input current	
	Automatically balances output capacitor bank	
Disadvantages	Requires input voltage state sensing	More strict EMI filtering
		Requires input voltage sensing
		Requires extra control loop to balance output capacitor bank
		More complex control algorithm

Table 2.1 - Comparison of Control Methods for the VIENNA Rectifier

In general, the VIENNA rectifier boasts a significant number of advantages over alternative rectifying circuits. These advantages include:

- Low input current harmonic distortion
- Three-level output for compatibility with any DC-DC converter
- Low switch count
- Low control effort in terms of quantity of required gate drives
- Compatibility with variable frequency inputs

2.2.2 DC-DC Step Down Conversion

Once the AC power from the wave generator is converted into DC power, it is concluded that it might be necessary to utilize DC-DC step-down conversion to reduce the DC power. In order to accomplish this, various methods of step-down conversion were investigated. These methods, along with applicable benefits and drawbacks, are discussed in this section.

Voltage Divider — A voltage divider is a simple, inexpensive tool that could be used to reduce DC power. For a voltage divider, the output voltage across the

load resistor is given by $V_o = V_i \times \frac{R_l}{R_l + R}$. This voltage divider is not ideal, as it is highly inefficient, resulting in a constant loss of power equal to $100 \times \left(1 - \frac{R_l}{R_l + R}\right)\%$. Also, the circuit itself does not contain any inherent control, so a separate circuit would need to be designed in order to provide control options.

Zener Regulator — A zener regulator has an additional degree of control provided by the zener diode. The zener diode allows current to pass in the reverse direction under certain conditions that would damage regular diodes, and it can be used to control the output voltage. For this circuit, the output voltage is given by $V_o = \frac{R_L(V_i - V_Z - RI_Z)}{R}$. This is not ideal for voltage regulation, because the zener voltage is dependent on the input voltage and on the load.

Series Voltage Regulator — Adding a common collector BJT to the zener regulator results in a series voltage regulator. The presence of the transistor reduces the load on the diode, reducing the fluctuation of zener voltage. This circuit has the capability to regulate a voltage drop with greater stability than the previously discussed regulators, but it is still dependant on the load. All of these regulators also run the risk of overheating if the difference between the input and output voltage is large.

Buck Converter — After researching different DC-DC converters, it was found that a basic voltage divider or a linear regulator would be extremely inefficient due to the power losses associated with it. Additionally, there are ripple currents and high ripple voltage, ΔVo, associated with these circuits. This phenomenon is greatly reduced by using dc-dc step-down converters (buck converter) with topologies that include high switching frequency. Research showed that the two most appropriate buck converter topologies for the design were: Asynchronous buck converter and Synchronous buck converter. The main difference between these two topologies is the difference in its design.

First topology is shown in Figure 2.5. This topology uses a buck convertor with a switch, diode, inductor and a capacitor. The diode in such a design is called a “free-wheeling” diode. This is because the diode eliminates or reduces any sort of fly-back voltage or voltage spikes in the inductive load as a result of sudden voltage drop in the supply voltage or if the supply voltage were to be completely removed.

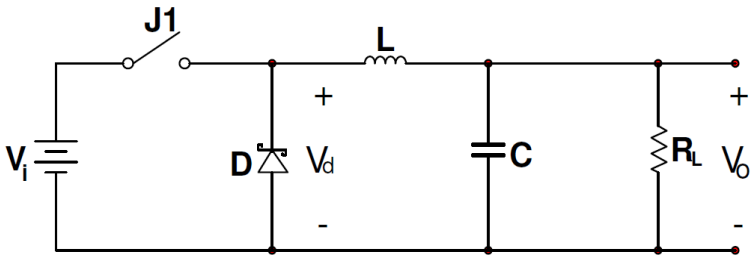


Figure 2.5 - Asynchronous Buck Converter

The second topology is shown in Figure 2.6. This topology uses a buck converter with a switch and the inner diode is replaced by another switch. Ideally, this switch would be a semiconductor transistor of type BJT or MOSFET. Generally, MOSFETs are considered to be a better option. This is because BJTs require an input current to turn on and causes offset. BJTs are more desirable for designs requiring fast switching as they lack gate capacitance; although, this is at an expense of lower efficiency. MOSFETs offer better switching frequency, higher efficiency and less complexity. Comparing between PMOS and NMOS, PMOS served as a better option as it is less complex in nature.

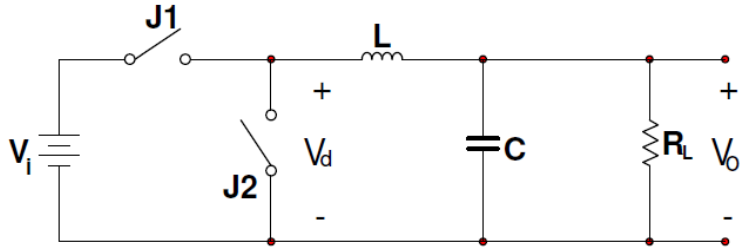


Figure 2.6 - Synchronous Buck Converter

Looking at the two topologies, it was critical to determine the most viable design. Table 2.2 provides a detailed comparison between the two:

Comparison	Asynchronous	Synchronous
1. Components	Uses a switch J1 (MOSFET) and diode D (Schottky Key)	Uses two switches J1 and J2 (MOSFETs)
2. Voltage Drop	Low forward voltage drop at the diode	Much lower voltage drop at the MOSFET
3. Power Dissipation	High	Low
4. Switching Losses	Low	Negligible
5. Switching Speed	Slow	Fast
6. Efficiency	High	Higher
7. Total Cost	Less expensive	More expensive

Table 2.2 - Comparison of Synchronous versus Asynchronous Converters

A mathematical comparison between the two could be made to further clarify the most appropriate topology for the design. Other than cost and complexity of the design, the most important factors that contribute mathematically to determine efficiency would include:

1. Duty Cycle (D) should be lower and
2. Output Voltage (V_o) must be higher to eliminate power dissipation losses

Realistic values were used in order to achieve goal-specific results. Accordingly, the parameter values for the design are as follows:

V_i = 70V, V_o = 12V, I_o = 2A

Utilizing basic equations for Duty Cycle and Power Loss, we can generate the values for the two topologies. At the given parameters, the voltage drop (V_d) for a Schottky diode is known to be around 0.4V while that for a MOSFET is 0.1V (for low-voltage devices). Table 2.3 shows a comparison of power losses for synchronous and asynchronous buck converters with equal duty cycles.

Topology	**% Duty Cycle (D) V_o/V_i x 100**	**Power Loss $V_d I_o(1-D)$**	**% Power Loss $V_d(1-D)/V_o$**
1. Asynchronous	17.14%	0.66 W	2.76%
2. Synchronous	17.14%	0.25W	0.69%

Table 2.3 - Comparison of Power Losses for Synchronous and Asynchronous Buck Converters

Similarly, the efficiency could also be compared as ~90% for asynchronous topology and ~94% for synchronous topology[1].

Looking at the comparison, the synchronous buck converter topology was chosen, neglecting its component cost which will be covered by the sponsor.

While the buck converter is a DC-DC step-down converter, combining a buck converter with a DC-DC step-up boost converter results in a buck-boost converter. This circuit can be used as either a step-up converter or a step-down converter, depending upon the duty cycle of the switching transistor.

2.2.3 Analog to Digital Signal Conversion

In order to transfer the power signal from the wave generator to the sensor package, it may be necessary to convert the signal from analog to digital. For this reason, conversion from analog to digital signal is researched. Analog to digital converters, or ADCs, typically consider the analog voltage or current input and convert the magnitude to a digital number. The output is generally a two's compliment binary number. These devices can vary significantly depending on the resolution, or the number of digital values that can be generated for an

analog input. Accuracy errors in ADCs are typically found in the least significant bit of the digital output, and may be the result of an aperture error. This particular error is of significant interest, as it results from clock jitter when converting time dependent analog signals to digital. Because the wave power is expected to vary with time, this error is likely to be encountered in conversion from analog to digital. The significance of the error depends on the resolution; increasing the quantity of bits in the digital output signal decreases the dependence on the least significant bit.

Analog to Digital Converters can be found in various forms. To determine the most suitable and accurate analog to Digital Converter, the first step is to determine the amount of bits required by the design. This can be determined by looking Table 2.4 which shows the resolution in ppm and dB for converter systems from 8 bits to 24 bits:

# of Bits	**2^n**	**LSB (FS = 1V)**	**Resolution (%)**	**Resolution (ppm)**	**Resolution (dB)**
8	256	3.91 mV	0.391	3910	48.16
10	1024	977 µV	0.0977	977	60.21
12	4096	244 µV	0.0244	244	72.25
14	16384	61 µV	0.0061	61	84.29
16	65536	15.3 µV	0.00153	15.3	96.33
18	262144	3.81 µV	0.000381	3.81	108.37
20	1048576	954 nV	9.54×10^{-5}	0.954	120.41
22	4194304	238 nV	2.38×10^{-5}	0.238	132.45
24	16777216	59.5 nV	5.95×10^{-6}	0.0595	144.46

Table 2.4 - Resolution amount for 8-Bit system to 24-Bit system

As seen in Table 2.4, high precision can be obtained by choosing the right number of bits. If the system requires a 21 bit converter, it is recommended to use 22 or 24 bit converter. This is just a precautionary measure as it allows the user to design a system that needs more bits, if necessary. An example of a circuit design for an ADC is depicted in Figure 2.4. This particular circuit design produces an 8-bit binary output from an analog input signal. The analog input is fed to a buffer amplifier at the CON-BNC connector, and the digital output leaves via the ADCV_DATA connector.

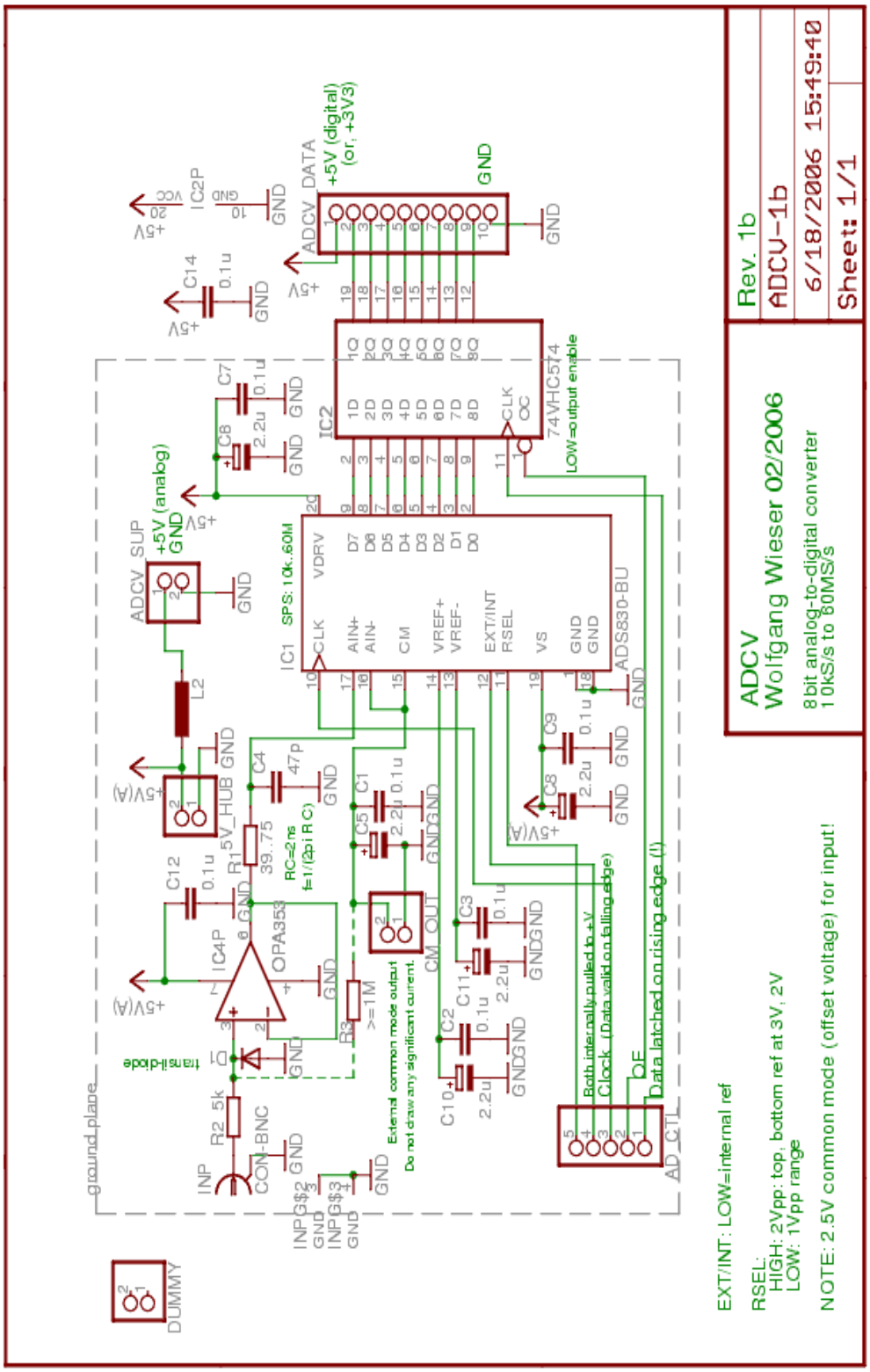


Figure 2.7 - 8-bit Analog to Digital Converter Circuit

2.2.4 MOSFET Driver

Among the possible devices that could serve as a switch for the buck converter with an LC filter, a metal oxide semiconductor field effect transistor (MOSFET) seemed ideal because of its capacity for high frequency switching, a capability that would improve the buck converter's ability to maintain a consistent output voltage. Several MOSFET drivers were investigated in order to find the best fit for this project, and they are discussed in this section.

The LM5101A 3A High Voltage High-Side and Low-Side Gate Driver from National Semiconductor is able to operate with an input voltage up to 100V, a supply voltage between 7.5V and 14V, and provide 3A of gate drive, with a listed price of $1.35 per unit per thousand [7]. The parameters for this device are given in Table 2.5.

Parameters	**Values**
Topology	Synchronous Buck, Bridge
Input Max Voltage	100 Volt
Supply Minimum	7.5 Volt
Supply Maximum	14 Volt
Peak Sink Current	3 Amp
Peak Source Current	3 Amp
Output Rise Time (tr)	10 ns
Output Fall Time (tf)	10 ns
Bottom Driver Prop Delay	25 ns
Top Driver Propagation Delay	25 ns
Pulse Width Min	50 ns
Quiescent Current	0.2 ma
High Side Drive	Yes
Low Side Drive	Yes
Outputs	2
Low Gate Enable	No
UVLO	Yes
Shut down	No
Internal Boot Diode	Yes
Input Control	Dual, independent
Special Features	TTL type threshold inputs
Reg Type	MOSFET Driver
Temperature Minimum	-40° C
Temperature Maximum	125° C

Table 2.5 - Parameters for the LM5101A Driver

The ADP3625 High Speed, Dual, 4A MOSFET Driver from Analog Devices is able to operate with a supply voltage between 4.5V and 18V, providing 4A of gate drive, with a listed price of $0.88 per unit per thousand [8]. These devices

also included internal temperature sensors with overheating shutdown at excessive junction temperatures. The parameters for this device are given in Table 2.6.

Parameters	**Values**
Product Description	High Speed, Dual, 4 Amp MOSFET Driver, inverting A & non-inv B input pins, 4.5V<Vin<18V
V_{in} Range (V)	4.5-18
Peak Drive Current (A)	4
Prop-Delay Rising (ns)	14
UVLO On/Off T-Hold V typ	4.2 / 3.9
Precision Enable	Yes
Over Temperature Protection	Yes
Over Temperature Warning Signal	Yes
Package	8L-MSOP_VD; 8L-SOIC-EP
Temperature Range (Deg C)	-40 to +85
Price* (1000 pcs.)	$0.88

Table 2.6 - Parameters for the ADP3625 Driver

The LTC4440-5 series of drivers from Linear Technology is able to operate with an input voltage up to 60V and a supply voltage between 4V and 15V, with an output of 1.1A and a listed price of $2.50 per unit, or $1.75 per unit per thousand [9]. The parameters for this device are given in Table 2.7.

Parameters	**Values**
Maximum Operating TS	60 V
Absolute Max TS	80 V
MOSFET Gate Drive	4 V to 15 V
V_{cc} UV^{+}	3.2 V
V_{cc} UV^{-}	3.04 V
INP Voltage	-0.3 V to 15 V
BOOST Voltage (continuous)	-0.3 V to 85 V
BOOST Voltage (100 ms)	-0.3 V to 95 V
TS Voltage (continuous)	-5 V to 70 V
TS Voltage (100 ms)	-5 V to 80 V
Peak Output Current < 1 µs (TG)	4A
Temperature Range (Deg C)	-40° C to 85° C
Junction Temperature	125° C

Table 2.7 - Parameters for the LTC4440-5 Driver

2.2.5 Controllers

A variety of system control options were considered to handle the control portion of the power conversion. Each of the available system controllers possessed

costs and benefits that needed to be weighed in order to make the best selection for this project. The costs and benefits of several controller systems are discussed in this section.

Field Programmable Gate Arrays — Field programmable gate arrays, or FPGAs, are integrated circuits that can be programmed by the consumer after manufacture. The ability of an FPGA to be individually programmed is a significant potential benefit, as other controllers programmed during manufacture lack flexibility. Another advantage to the FPGA is the ability to define and simulate the exact code before programming the device. One potential disadvantage is that FPGAs often occupy more space than other controller systems.

Microcontrollers — A microcontroller is a miniature computer built on an integrated circuit. One advantage to a microcontroller is their very small power consumption, particularly while inactive. Microcontrollers contain their own memory that may be field programmable or defined during manufacture. They are also typically very small, which can be a significant advantage when space conservation is an issue. Microcontrollers are also readily available on the market and generally inexpensive.

Digital Signal Processors — Digital Signal Processors, or DSPs, are a variety of microprocessor designed primarily for digital signal processing, but they often provide other features, sometimes serving as microcontrollers. Like embedded microcontrollers, they are small and often, though not invariably, inexpensive.

PIC Microcontrollers — PIC microcontrollers derive their name from Programmable Interface Controller. Some of the many benefits of PIC microcontrollers include low cost, high availability, a large number of users that has resulted in a large quantity of documentation and application notes, programming capability, low power consumption, and the capability to enter a low-power sleep state. Some of the potential drawbacks include a limited number of instructions, ranging from 35 to 80 or more, or only a single accumulator [10]. These drawbacks do not necessarily apply strictly to all PIC microcontrollers. With a very wide range of available options, a PIC microcontroller can feasibly be obtained for nearly any application desired.

A variety of PIC microcontrollers available from Microchip were investigated in order to find the best fit for this project, and they are discussed in this section.

The PIC10F222 is an inexpensive, 8-bit static Flash-based microcontroller. It uses 33 single-word / single-cycle 12-bit wide instructions. Some of its features include low power sleep current, in-circuit debugging support, and programmable code protection. The parameters for this device are given in Table 2.8.

Parameters	Values
Program Memory Type	Flash
Program Memory (KB)	0.75
Program Memory KWords	0.5
Self-Write	No
CPU Speed (MIPS)	2
RAM Bytes	23
Max CPU Speed (MHz)	8
Internal Oscillator	4 MHz, 8 MHz
Timers	1 x 8-bit
ADC	2 ch, 8-bit
Temperature Range (deg C)	-40 to 125
Operating Voltage Range (V)	2 to 5.5
Input / Output Pins	4
Pin Count	6
Cap Touch Channels	2
Volume Pricing	$0.39

Table 2.8 - Parameters for the PIC10F222 Microcontroller

The PIC16F886 is an inexpensive PIC microcontroller that features on-board EEPROM data memory, an analog comparator, an internal oscillator with selectable 8 MHz – 32 KHz, and programmable on-chip voltage reference. The parameters for this device are given in Table 2.9.

Parameters	Values
Program Memory Type	Flash
Program Memory (KB)	3.5
Program Memory KWords	2
Self-Write	No
CPU Speed (MIPS)	5
RAM Bytes	128
Data EEPROM (bytes)	256
Max CPU Speed (MHz)	20
Internal Oscillator	8 MHz, 32 kHz
Timers	2 x 8-bit, 1 x 16-bit
ADC	4 ch, 10-bit
Comparators	1
Temperature Range (deg C)	-40 to 125
Operating Voltage Range (V)	2 to 5.5
Input / Output Pins	6
Pin Count	8
Cap Touch Channels	3
Volume Pricing	$0.91

Table 2.9 - Parameters for the PIC12F683 Microcontroller

The PIC16F886 is an 8-bit Flash-based CMOS PIC microcontroller with features that include self-programming, two comparators, a power saving sleep mode, and in-circuit debugging. The parameters for this device are given in Table 2.10.

Parameters	**Values**
Program Memory Type	Flash
Program Memory (KB)	14
Program Memory KWords	8
Self-Write	Yes
CPU Speed (MIPS)	5
RAM Bytes	368
Data EEPROM (bytes)	256
Max CPU Speed (MHz)	20
Internal Oscillator	8 MHz, 32 kHz
Digital Communication Peripherals	1-A/E/USART, 1-MSSP(SPI/I2C)
Capture/Compare/PWM Peripherals	1 CCP, 1 ECCP
Timers	2 x 8-bit, 1 x 16-bit
ADC	4 ch, 10-bit
Comparators	2
Temperature Range (deg C)	-40 to 125
Operating Voltage Range (V)	2 to 5.5
Input / Output Pins	6
Pin Count	28
Cap Touch Channels	11
Volume Pricing	$1.49

Table 2.10 - Parameters for the PIC16F886 Microcontroller

The PIC18F2620 is an 8-bit Flash-based CMOS PIC microcontroller with features that include a failsafe clock monitor, two comparators, run, idle, and sleep modes, and C compiler optimized RISC architecture. The parameters for this device are given in Table 2.11.

Parameters	**Values**
Program Memory Type	Flash
Program Memory (KB)	64
Program Memory KWords	32
Self-Write	Yes
CPU Speed (MIPS)	10
RAM Bytes	3968
Data EEPROM (bytes)	1024
Max CPU Speed (MHz)	40
Internal Oscillator	8 MHz, 32 kHz
Digital Communication Peripherals	1-A/E/USART, 1-MSSP(SPI/I2C)
Capture/Compare/PWM Peripherals	2 CCP
Timers	1 x 8-bit, 3 x 16-bit

ADC	10 ch, 10-bit
Comparators	2
Temperature Range (deg C)	-40 to 125
Operating Voltage Range (V)	2 to 5.5
Input / Output Pins	25
Pin Count	28
Volume Pricing	$4.06

Table 2.11 - Parameters for the PIC18F2620 Microcontroller

The dsPIC33FJ16GS504 is a 16-bit digital signal controller with features that include a failsafe clock monitor, two high speed analog comparators, run, idle, and sleep modes, and C compiler optimized instruction set. The parameters for this device are given in Table 2.12.

Parameters	**Values**
Program Memory Type	Flash
Program Memory (KB)	16
Program Memory KWords	32
Self-Write	Yes
CPU Speed (MIPS)	40
RAM Bytes	2048
Data EEPROM (bytes)	0
Max CPU Speed (MHz)	40
Internal Oscillator	7.37 MHz, 32 kHz
nanoWatt Features	Fast Wake/Fast Control
Digital Communication Peripherals	1-UART, 1-SPI, 1-I2C
Analog Peripherals	2-A/D 12x10-bit @ 4000(ksps) 4-D/A 1x10-bit @ 640(ksps)
Timers	2 x 16-bit
16-bit PWM resolutions	16
Motor Control PWM Channels	8
Comparators	4
Temperature Range (deg C)	-40 to 125
Operating Voltage Range (V)	3 to 3.6
Input / Output Pins	35
Pin Count	44
Volume Pricing	$3.42

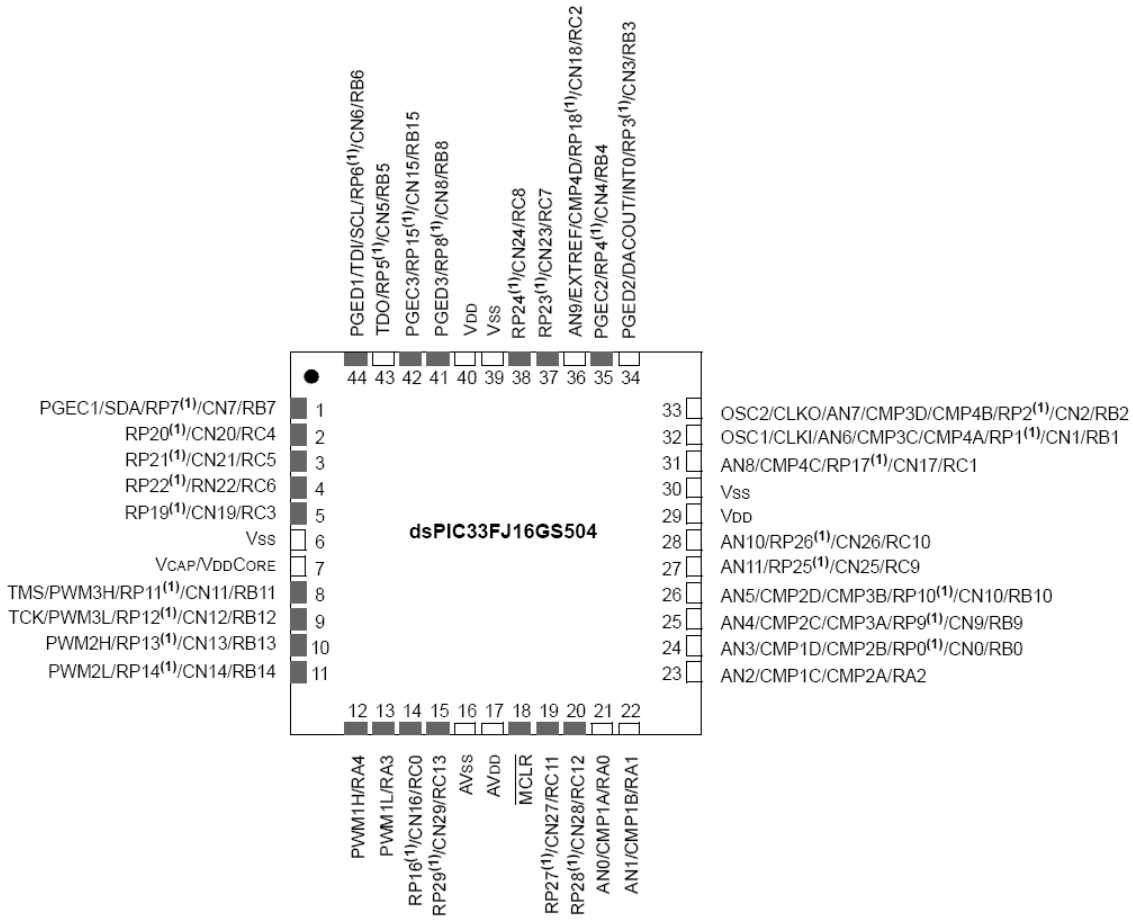
Table 2.12 - Parameters for the dsPIC33FJ16GS504 Microcontroller

The PIC microcontroller was determined to be the most appropriate choice for this project. PIC microcontrollers are readily available with a wide array of available parameters making them a good fit for many applications. They are inexpensive and highly versatile. For the purposes of this project, the 16-bit dsPIC33FJ16GS504 microcontroller was determined to be the optimal choice for its low cost, programmability with the C programming language, four

comparators, power saving features, and high maximum CPU speed. The pin layout for this device is shown in Figure 2.8.

44-Pin QFN(2)

■ = Pins are up to 5V tolerant



Note 1: The RPn pins can be used by any remappable peripheral. See the **"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Controller Families"** table for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to connect to Vss externally.

Figure 2.8 - Pin Layout for the dsPIC33FJ16GS504 PIC Microcontroller (Permission requested from Microchip)

Descriptions for the pin inputs and outputs for the dsPIC33FJ16GS504 PIC are given in Figure 2.9 and Figure 2.10.

Pin Name	Pin Type	Buffer Type	PPS Capable	Description
CMP1A	I	Analog	No	Comparator 1 Channel A
CMP1B	I	Analog	No	Comparator 1 Channel B
CMP1C	I	Analog	No	Comparator 1 Channel C
CMP1D	I	Analog	No	Comparator 1 Channel D
CMP2A	I	Analog	No	Comparator 2 Channel A
CMP2B	I	Analog	No	Comparator 2 Channel B
CMP2C	I	Analog	No	Comparator 2 Channel C
CMP2D	I	Analog	No	Comparator 2 Channel D
CMP3A	I	Analog	No	Comparator 3 Channel A
CMP3B	I	Analog	No	Comparator 3 Channel B
CMP3C	I	Analog	No	Comparator 3 Channel C
CMP3D	I	Analog	No	Comparator 3 Channel D
CMP4A	I	Analog	No	Comparator 4 Channel A
CMP4B	I	Analog	No	Comparator 4 Channel B
CMP4C	I	Analog	No	Comparator 4 Channel C
CMP4D	I	Analog	No	Comparator 4 Channel D
DACOUT	O	—	No	DAC output voltage
ACMP1-ACMP4	O	—	Yes	DAC trigger to PWM module
EXTREF	I	Analog	No	External voltage reference input for the reference DACs
REFCLKO	O	—	Yes	REFCLKO output signal is a postscaled derivative of the system clock
FLT1-FLT8	I	ST	Yes	Fault Inputs to PWM module
SYNCI1-SYNCI2	I	ST	Yes	External synchronization signal to PWM Master Time Base
SYNCO1	O	—	Yes	PWM master time base for external device synchronization
PWM1L	O	—	No	PWM1 low output
PWM1H	O	—	No	PWM1 high output
PWM2L	O	—	No	PWM2 low output
PWM2H	O	—	No	PWM2 high output
PWM3L	O	—	No	PWM3 low output
PWM3H	O	—	No	PWM3 high output
PWM4L	O	—	Yes	PWM4 low output
PWM4H	O	—	Yes	PWM4 high output
PGED1	I/O	ST	No	Data I/O pin for programming/debugging communication Channel 1
PGEC1	I	ST	No	Clock input pin for programming/debugging communication Channel 1
PGED2	I/O	ST	No	Data I/O pin for programming/debugging communication Channel 2
PGEC2	I	ST	No	Clock input pin for programming/debugging communication Channel 2
PGED3	I/O	ST	No	Data I/O pin for programming/debugging communication Channel 3
PGEC3	I	ST	No	Clock input pin for programming/debugging communication Channel 3
$\overline{MCLR}$	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	No	Ground reference for analog modules
VDD	P	—	No	Positive supply for peripheral logic and I/O pins
VCAP/VDDCORE	P	—	No	CPU logic filter capacitor connection
VSS	P	—	No	Ground reference for logic and I/O pins

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; I = Input
ST = Schmitt Trigger input with CMOS levels; P = Power; O = Output
TTL = Transistor-Transistor Logic; PPS = Peripheral Pin Select

Figure 2.9 - Pin Description for the dsPIC33FJ16GS504 PIC Microcontroller (Permission requested from Microchip)

Pin Name	Pin Type	Buffer Type	PPS Capable	Description
AN0-AN11	I	Analog	No	Analog input channels
CLKI	I	ST/CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
CN0-CN29	I	ST	No	Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
IC1-IC2	I	ST	Yes	Capture inputs 1/2
OCFA	I	ST	Yes	Compare Fault A input (for Compare Channels 1 and 2)
OC1-OC2	O	—	Yes	Compare Outputs 1 through 2
INT0	I	ST	No	External Interrupt 0
INT1	I	ST	Yes	External Interrupt 1
INT2	I	ST	Yes	External Interrupt 2
RA0-RA4	I/O	ST	No	PORTA is a bidirectional I/O port
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port
RC0-RC13	I/O	ST	No	PORTC is a bidirectional I/O port
RP0-RP29	I/O	ST	No	Remappable I/O pins
T1CK	I	ST	Yes	Timer1 external clock input
T2CK	I	ST	Yes	Timer2 external clock input
T3CK	I	ST	Yes	Timer3 external clock input
$\overline{\text{U1CTS}}$	I	ST	Yes	UART1 clear to send
$\overline{\text{U1RTS}}$	O	—	Yes	UART1 ready to send
U1RX	I	ST	Yes	UART1 receive
U1TX	O	—	Yes	UART1 transmit
SCK1	I/O	ST	Yes	Synchronous serial clock input/output for SPI1
SDI1	I	ST	Yes	SPI1 data in
$\overline{\text{SDO1}}$	O	—	Yes	SPI1 data out
$\overline{\text{SS1}}$	I/O	ST	Yes	SPI1 slave synchronization or frame pulse I/O
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1
TMS	I	TTL	No	JTAG Test mode select pin
TCK	I	TTL	No	JTAG test clock input pin
TDI	I	TTL	No	JTAG test data input pin
TDO	O	—	No	JTAG test data output pin

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; I = Input
ST = Schmitt Trigger input with CMOS levels; P = Power; O = Output
TTL = Transistor-Transistor Logic; PPS = Peripheral Pin Select

Figure 2.10 - Pin Description for the dsPIC33FJ16GS504 PIC Microcontroller (Permission requested from Microchip)

Further investigation into the functioning of the dsPIC33FJ16GS504 microcontroller was required in order to ensure that the desired results were achieved, and to protect the microcontroller from potential damage. Microchip provided ample information regarding the proper use of their microcontroller. The basic requirements of the dsPIC33FJ16GS504 microcontroller are further expanded below.

Decoupling Capacitors: Decoupling capacitors are required on every power supply pin. These include the V_{DD}, V_{SS}, AV_{DD}, and AV_{SS} pins. Several factors needed to be considered in choosing the appropriate capacitor. Microchip recommended the use of a ceramic capacitor of 0.1 µF, 10–20 V, with a resonance frequency over 20 MHz. These capacitors should be placed as close to the pin as possible, preferably within 6 mm on the same side of the board as the device. For the reduction of noise over 10 MHz, a second ceramic capacitor could be added, in parallel with the first, with a capacitance between 0.01 µF and 0.001 µF. Figure 2.11 shows the recommended minimum connections for the decoupling capacitors.

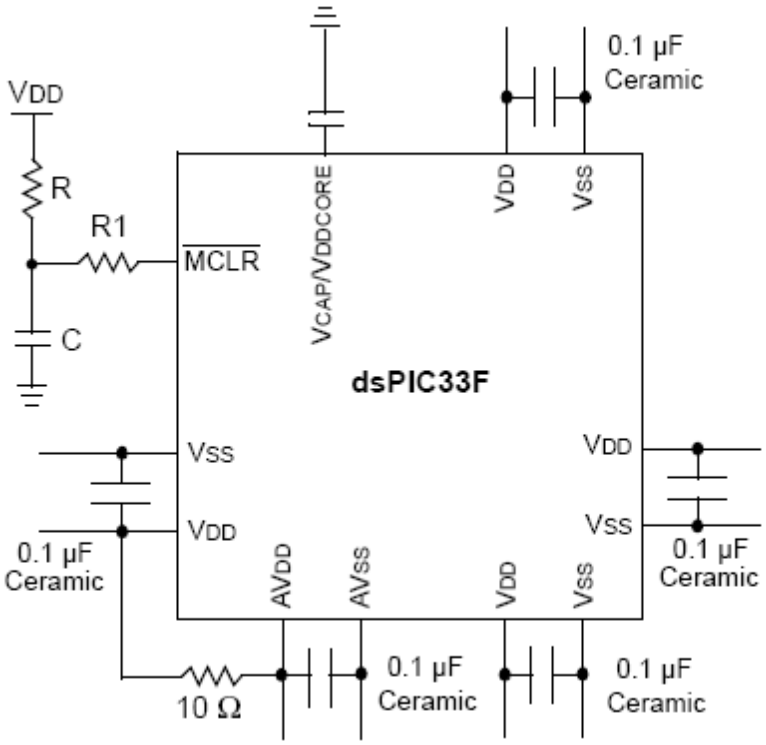


Figure 2.11 - Minimum Recommended Connections for Decoupling Capacitors for the dsPIC33FJ16GS504 PIC Microcontroller
(Permission requested from Microchip)

Capacitor on Internal Voltage Regulator: For the V_{CAP}/V_{DDCORE} pin, a capacitor with low ESR, under 5 Ω, is needed to make the output voltage on the voltage regulator stable. Microchip recommended a ceramic or tantalum capacitor between 4.7 µF and 10 µF, 16V connected to ground, placed within 6 mm of the pin.

Master Clear Pin: This pin is used for resetting the microcontroller, as well as for programming and debugging. Differing values of resistance and capacitance need to be placed on the pin depending on the current status of the

microcontroller. While programming and debugging the microcontroller, Microchip recommends that the capacitance be isolated from the master clear pin. Figure 2.12 shows the recommended connection for the master clear pin.

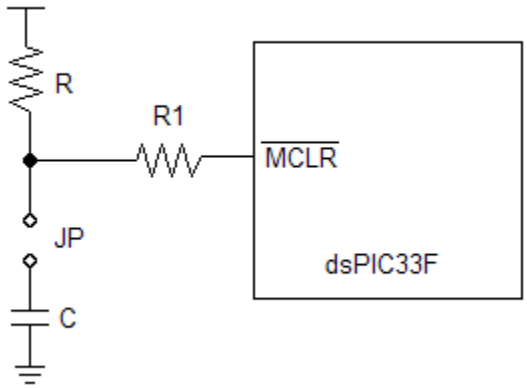


Figure 2.12 - Recommended Connection for the Master Clear Pin for the dsPIC33FJ16GS504 PIC Microcontroller

ICSP Pins: In-Circuit Serial Programming pins, such as the PGECx and PGEDx pins, are used for programming and debugging. Microchip advised against the use of pull-up resistors, series diodes, or capacitors in these pins, as this would interfere with the devices' communications for programming and debugging. IN the event that these components are required for the device, they should be removed during programming and debugging.

External Oscillator Pins: The dsPIC33FJ16GS504 microcontroller has both a high-frequency and a low-frequency oscillator. Microchip recommends that the circuit for the oscillator be placed on the same side of the board as the device, within 12 mm of the appropriate oscillator pin. They also suggested placing a grounded copper pour around the oscillator circuitry to separate it from any other nearby circuits. This copper pour needs to be routed to the MCU ground directly, and no power or signal traces should be run through it. Figure 2.13 shows the recommended placement of the oscillator circuit.

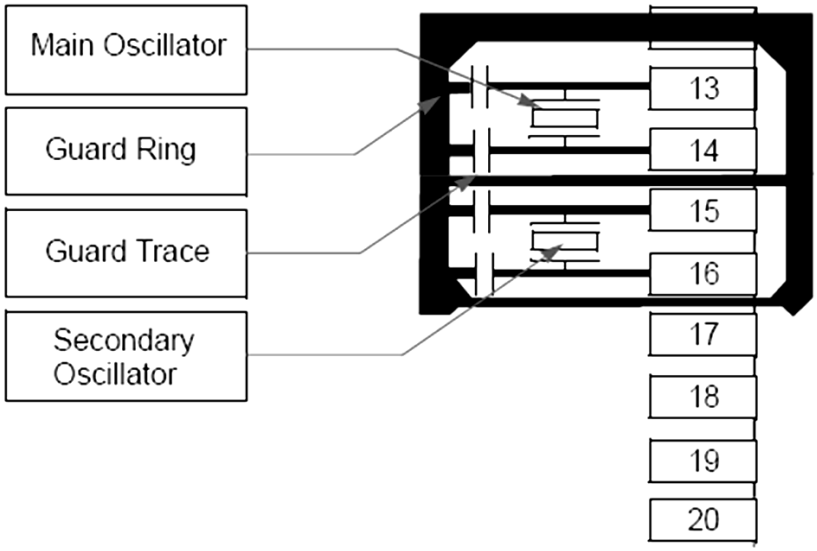


Figure 2.13 - Recommended Placement of the Oscillator Circuit for the dsPIC33FJ16GS504 PIC Microcontroller
(Permission requested from Microchip)

Oscillator Value Conditions on Device Start-Up: When the device first powers up, if the PLL is enabled and configured, the maximum oscillator source frequency must be constrained between 4 MHz and 8MHz. Otherwise, default settings will violate the device operating speed.

Configuration of Analog and Digital Pins During ICSP Operations: MPLAB ICD 2, ICD 3, or REAL ICE can be used as a debugger to automatically initialize all of the ANx pins as digital. The bits contained in the registers correlating to these A/D input pins that are initialized in this way must not be cleared by user application firmware, or else there will be communication errors between the debugger and the microcontroller. Furthermore, if MPLAB ICD 2, ICD 3, or REAL ICE are used as programmers, the ADPCFG registers must be configured correctly. Only debugging, and not programming, results in these registers being initialized. If the registers are not correctly configured, the A/D pins will be recognized as analog input pins, which could adversely affect the functionality.

Unused I/Os: I/O pins that are not going to be used should either be configured as outputs and driven to a logic-low state, or else connected to a resistor between 1 kΩ and 10 kΩ and connected to V_{SS}.

When the microcontroller is configured correctly, it can be used for a wide range of applications. Figure 2.14 shows the use of a dsPIC33FJ06GS202 microcontroller, in the same family of microcontrollers as the dsPICFJ06GS504, in a synchronous buck converter circuit.

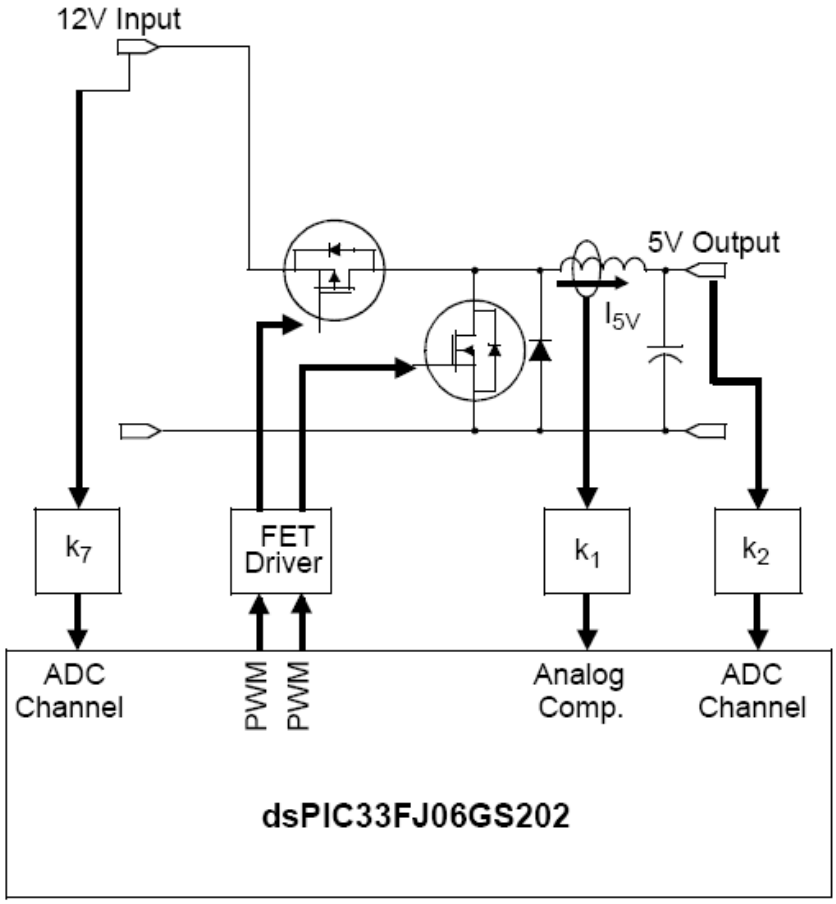


Figure 2.14 - Synchronous Buck Converter Circuit with dsPIC33FJ06GS202 PIC Microcontroller (Permission requested from Microchip)

CPU: The CPU module for the dsPIC33FJ16GS504 microcontroller utilizes 16-bit Harvard architecture and a 24-bit instruction word. All instructions for this device are executed in a single cycle except for instructions that alter the program flow, the double-word move instruction, and table instructions. DO and REPEAT instructions can be used for program loops and are interruptible at any time. The CPU features both MCU and DSP instructions, designed for compatibility with C compilers. Figure 2.15 shows a block diagram of the CPU for the dsPIC33FJ06GS202 microcontroller.

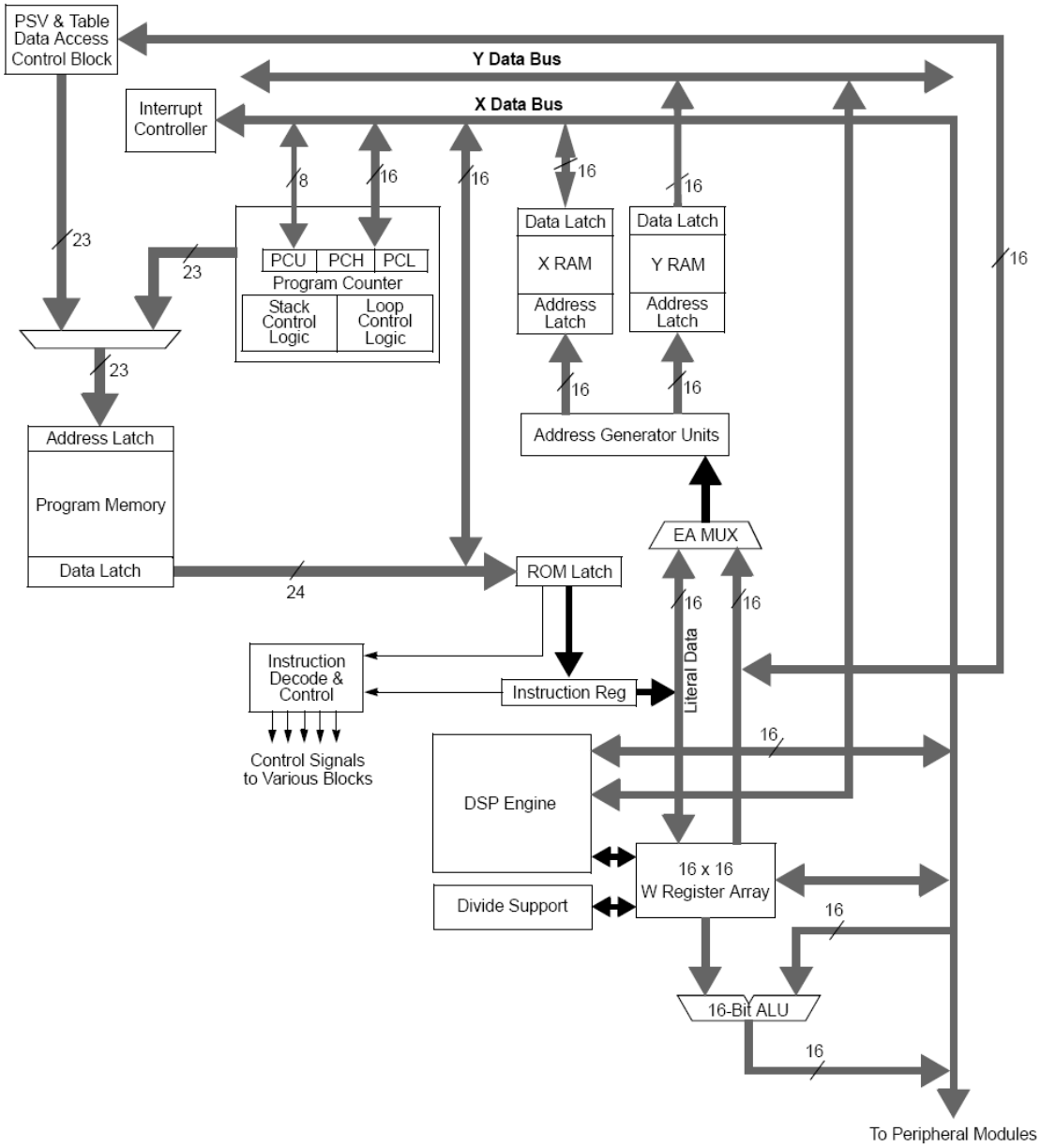


Figure 2.15 - CPU Block Diagram for the dsPIC33FJ16GS504 PIC Microcontroller (Permission requested from Microchip)

Figure 2.16 elaborates with a programmer's model for the CPU. Data space can be addressed either as 32K words or as 64 Kb. It is split into two sections which have been designated X and Y data memory, each with an independent Address Generation Unit. MCU instructions operate only through the X AGU, while DSP instructions may operate through the X or Y AGUs. The DSP engine includes a high-speed 17x17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators, and a 40-bit bidirectional barrel shifter that can shift a 40-bit value as many as 16 bits to the right or left in a single cycle.

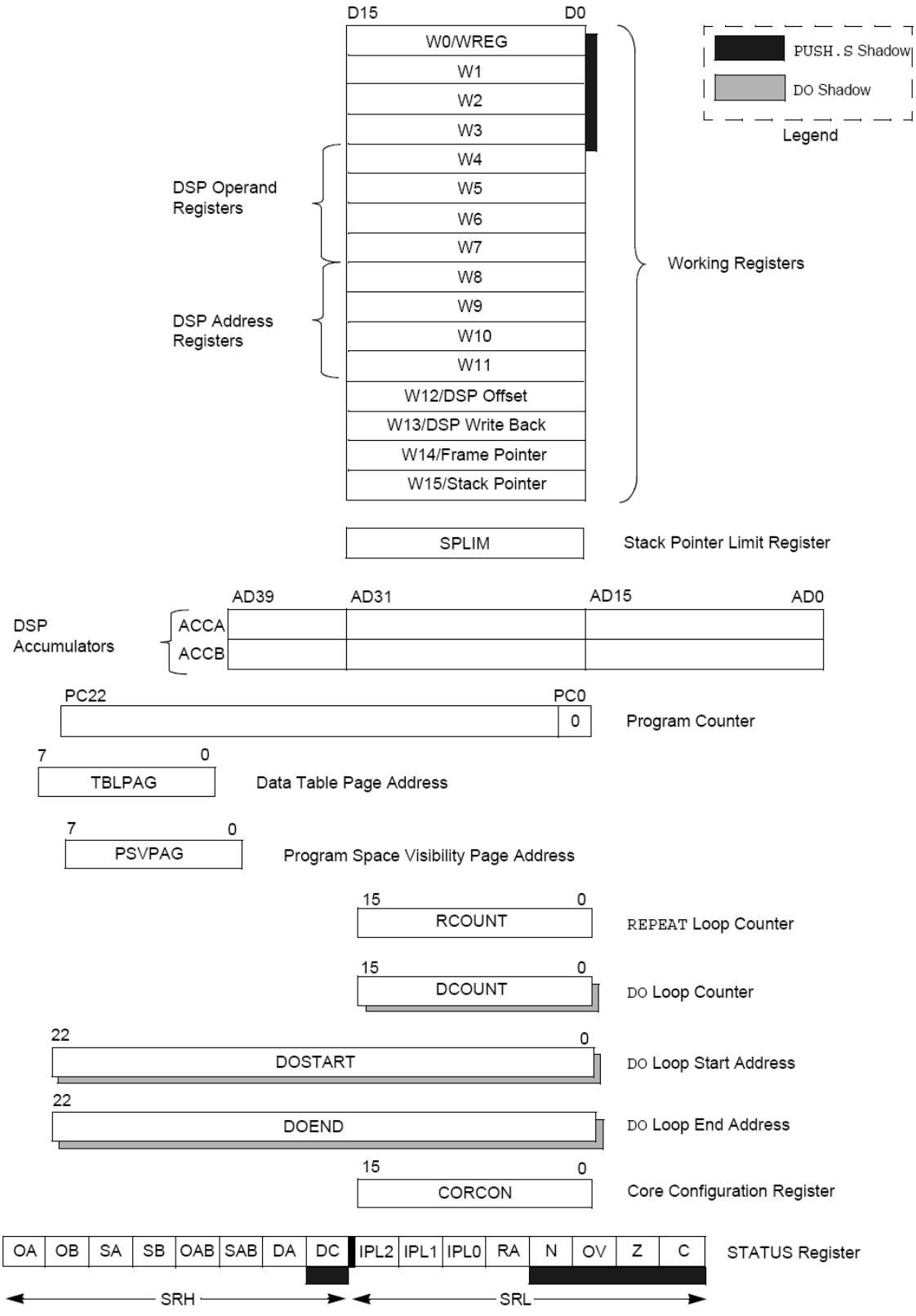
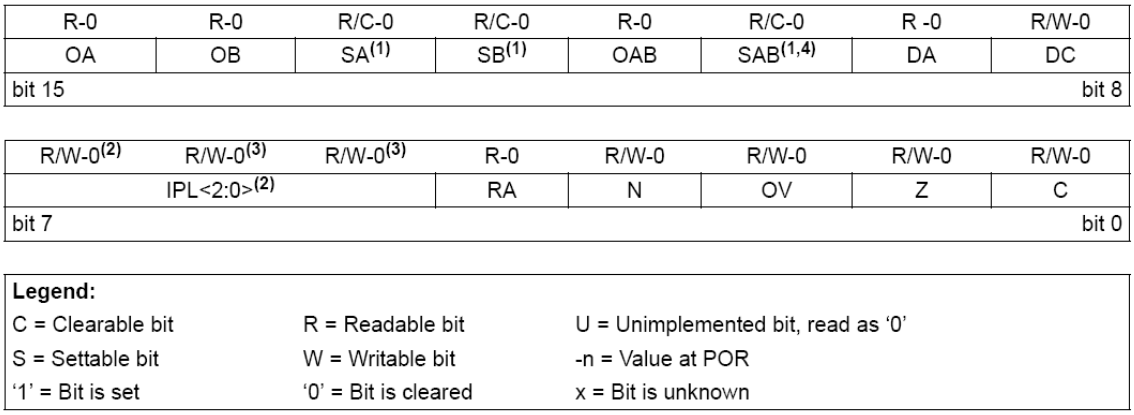


Figure 2.16 - CPU Programmer's Model for the dsPIC33FJ16GS504 PIC Microcontroller (Permission requested from Microchip)

Figure 2.17 depicts the designation of the CPU status register. Bit 15 (OA) is the Accumulator A Overflow Status bit, which holds a 1 if accumulator A has overflowed, else a 0. Bit 14 (OB) is the Accumulator B Overflow Status bit, which holds a 1 if accumulator B has overflowed, else a 0. Bit 13 (SA) is the Accumulator A Saturation 'Sticky' Status bit, which holds a 1 if accumulator A is or has been saturated, else a 0. Bit 12 (SB) is the Accumulator B Saturation 'Sticky' Status bit, which holds a 1 if accumulator B is or has been saturated, else a 0. Bit 11 (OAB) is the OA / OB Combined Accumulator Overflow Status bit, which holds a 1 if accumulators A or B have overflowed, else a 0. Bit 10 (SAB) is the SA / SB Combined Accumulator 'Sticky' Status bit, which holds a 1 if accumulators A or B are or have been saturated, else a 0. Bit 9 (DA) is the DO Loop Active bit, which holds a 1 if a DO loop is in progress, else a 0. Bit 8 (DC) is the MCU ALU Half Carry/Borrow bit a carry out form the 4th or 8th low-order bit of the result occurred, else a 0. Bits 7-5 (IPL<2:0>) are the CPU Interrupt Priority Status bits, forming a 3-bit binary bus defining the CPU Interrupt Priority Level ranging from 111 (Level 7) to 000 (Level 0). Bit 4 (RA) is the REPEAT Loop Active bit, holding a 1 if a REPEAT loop is in progress, else a 0. Bit 3 (N) is the MCU ALU Negative bit, holding a 1 if a negative result was obtained, else a 0. Bit 2 (OV) is the MCU ALU Overflow bit, holding a 1 if overflow occurred for signed arithmetic, else a 0. Bit 1 (Z) is the MCU ALU Zero bit, holding a 1 if an operation affecting the Z bit has set it at some point, else a 0 if the most recent operation affecting the Z bit cleared it. Bit 0 (C) is the MCU ALU Carry/Borrow bit, holding a 1 if a carry out occurred from the MSB of the result, else a 0.



R-0	R-0	R/C-0	R/C-0	R-0	R/C-0	R -0	R/W-0
OA	OB	SA(1)	SB(1)	OAB	SAB(1,4)	DA	DC
bit 15							bit 8

R/W-0(2)	R/W-0(3)	R/W-0(3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL<2:0>(2)			RA	N	OV	Z	C
bit 7							bit 0

Legend:		
C = Clearable bit	R = Readable bit	U = Unimplemented bit, read as '0'
S = Settable bit	W = Writable bit	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Figure 2.17 - CPU Status Register Designation for the dsPIC33FJ16GS504 PIC Microcontroller (Permission requested from Microchip)

Figure 2.18 depicts the designation of the core control register. Bits 15-13 are unimplemented. Bit 12 (US) is the DSP Multiply Unsigned/Signed Control bit, holding a 1 if the DSP engine multiplies are unsigned, else a 0. Bit 11 (EDT) is the Early DO Loop Termination Control bit, where holding a 1 terminates execution of the DO loop at the end of the current iteration, and holding a 0 does nothing. Bits 10-8 (DL<2:0>) are the DO Loop Nesting Level Status bits, which

comprise a 3-bit binary bus where the binary value defines the number of active DO loops, from 111 (7 DO loops active) to 000 (0 DO loops active). Bit 7 (SATA) is the ACCA Saturation Enable bit, which holds a 1 if accumulator A has saturation enabled, else a 0. Bit 6 (SATB) is the ACCB Saturation Enable bit, holding a 1 if accumulator B has saturation enabled, else a 0. Bit 5 (SATDW) is the Data Space Write from DSP Engine Saturation Enable bit, holding a 1 if the data space write has saturation enabled, else a 0. Bit 4 (ACCSAT) is the Accumulator Saturation Mode Select bit, holding a 1 for super saturation of 9.31, else 0 for normal saturation of 1.31. Bit 3 (IPL3) is the CPU Interrupt Priority Level Status bit, which holds 1 if the CPU interrupt priority level is greater than 7, else a 0. Bit 2 (PSV) is the Program Space Visibility in Data Space Enable bit, holding a 1 if program space is visible in data space, else a 0. Bit 1 (RND) is the Rounding Mode Select bit, holding a 1 if conventional biased rounding is enables, else a 0 if convergent unbiased rounding is enabled. Bit 0 (IF) is the Integer or Fractional Multiplier Mode Select bit, which holds a 1 if integer mode is enabled for DSP multiply operations, else a 0 if fractional mode is enabled for DSP multiply operations.

U-0	U-0	U-0	R/W-0	R/W-0	R-0	R-0	R-0
—	—	—	US	EDT(1)	DL<2:0>		
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3(2)	PSV	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	-n = Value at POR	'1' = Bit is set
0' = Bit is cleared	'x = Bit is unknown	U = Unimplemented bit, read as '0'	

Figure 2.18 - Core Control Register Designation for the dsPIC33FJ16GS504 PIC Microcontroller (Permission requested from Microchip)

ALU: The ALU on the dsPIC33FJ16GS504 PIC microcontroller has a width of 16 bits and is able to perform addition, subtraction, bit shifts, and logic operations. It uses 2's compliment for arithmetic operations. The ALU can operate on data from the W register array or from data memory, and ALU output can likewise be written to either of these locations. The ALU is also able to perform the following multiplication operations:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed by 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

It can also perform the following division operations:

- 32-bit signed / 16-bit signed
- 32-bit unsigned / 16-bit unsigned
- 16-bit signed / 16-bit signed
- 16-bit unsigned / 16-bit unsigned

DSP Engine: The dsPIC33FJ16GS504 utilizes a DSP engine with a 17-bit x 17-bit multiplier, a barrel shifter, and a 40-bit adder/subtractor. Generally, as the microcontroller uses single-cycle instruction flow architecture, the DSP engine and the MCU instruction flow cannot be simultaneously active. DSP engine options can be selected via the CPU Core Control register for multiplication, rounding, or saturation control. Figure 2.19 shows the block diagram for the DSP engine.

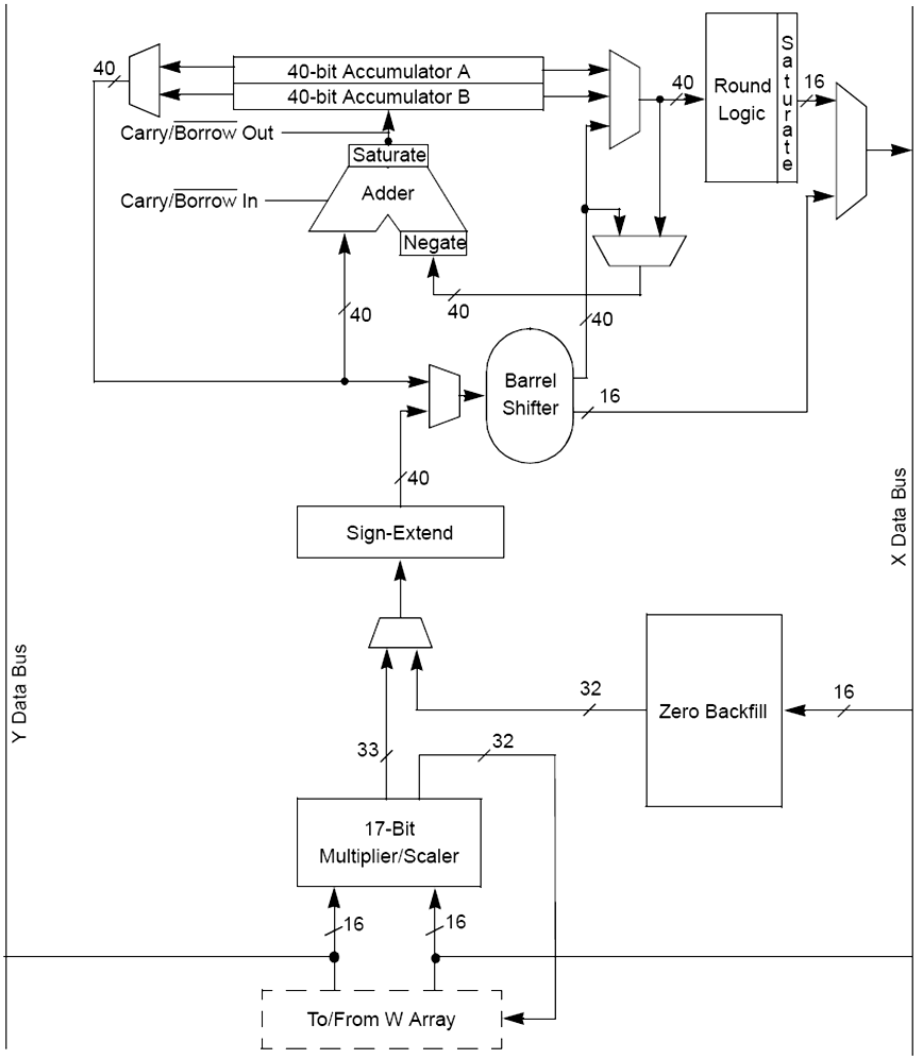


Figure 2.19 - DSP Engine Block Diagram for the dsPIC33FJ16GS504 PIC Microcontroller (Permission requested from Microchip)

Memory Organization: The dsPIC33FJ16GS504 microcontroller utilizes distinct program and memory data spaces, permitting access to program memory while code is being executed. Program memory space is accessible only to the lower half of the address range, form 0x000000 to 0x7FFFFF, with the exception of the TBLRD and TBLWT operations. Figure 2.20 shows the program memory map for the device.

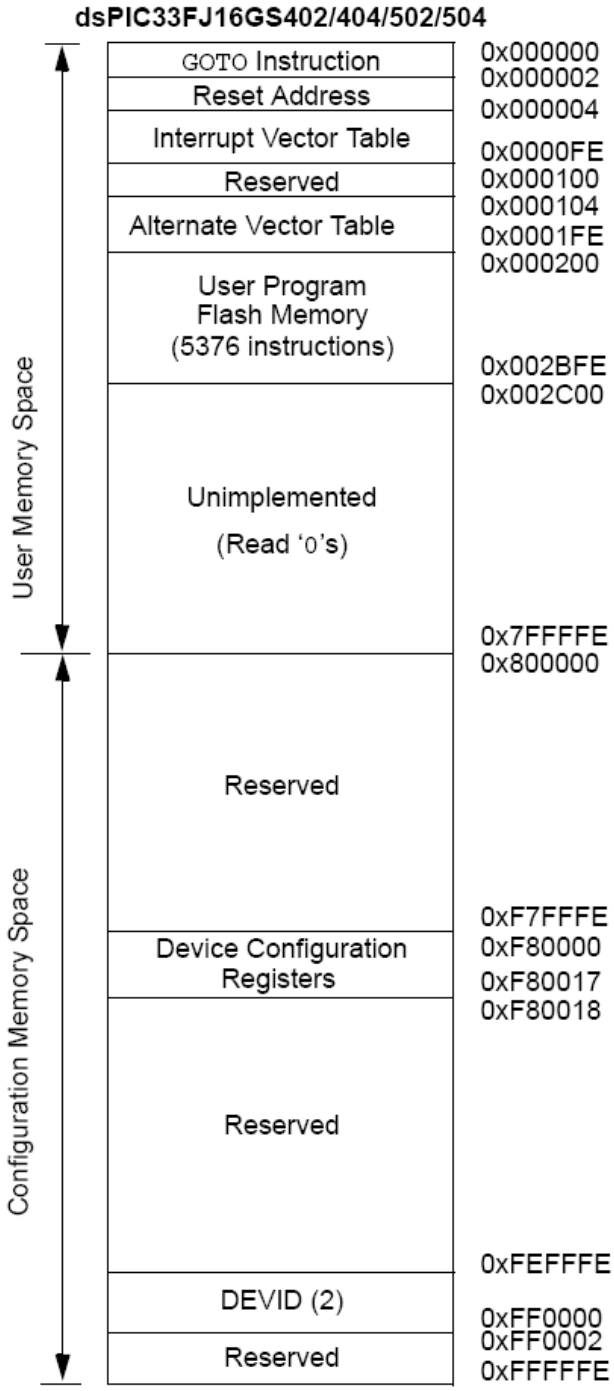


Figure 2.20 - Program Memory Map for the dsPIC33FJ16GS504 PIC Microcontroller (Permission requested from Microchip)

Program memory space is separated into word-addressable blocks, each 24 bits wide, which can be interpreted as a lower word and an upper word. The highest byte of the upper word (corresponding to bits 24-31) is never implemented. The addresses between 0x000000 and 0x000200 are held for hard-coded program execution vectors.

Addresses in the data memory space are 16 bits wide and point to data space, resulting in a 64Kb data space. The lower half corresponds to implemented memory addresses and the upper half to the Program Space Visibility area.

Flash Program Memory: The dsPIC33FJ16GS504 microcontroller utilizes internal Flash memory in order to store and execute code. It is possible to read, write, or erase memory during operation of the device. Flash memory can be programmed by either in-circuit serial programming or run-time self-programming. The former makes possible the manufacture of boards with unprogrammed devices that have the digital signal controller programmed immediately before shipping. The latter uses the table read and table write instructions to write program memory data in blocks of 64 instructions.

The device's programming time depends upon the values of the FRC accuracy (which is temperature dependant) and the FRC Oscillator Tuning register. It is given by the following equation:

$$T_{RW} = \frac{T}{7.37\ MHz\ \times (FRC\ Accuracy)\%\ \times (FRC\ Tuning)\%}$$

The process of programming the Flash memory entails programming one row at a time, according to the following algorithm:

1. Read eight rows of program memory. Store in data RAM.
2. Update program data in RAM with desired data.
3. Erase the block:
    a. Set NVMOP to 0010 to configure for erase. Set the ERASE and WREN bits.
    b. Write the starting address to be erased into TBLPAG and W.
    c. Write 0x55 to NVMKEY.
    d. Write 0xAA to NVMKEY.
    e. Set WR to start the erase cycle, stalling the CPU. WR is cleared when the erase completes.
4. Write the first 64 instructions from data RAM into program memory buffers.
5. Write the program block to Flash memory:
    a. Set NVMOP to 0001 to configure for programming. Clear the ERASE bit and set the WREN bit.
    b. Write 0x55 to NVMKEY.

c. Write 0XAA to NVMKEY.
d. Set WR to start the programming cycle, stalling the CPU

6. Repeat from 4, incrementing TBLPAG, until all 512 instructions have been written to Flash memory.

Oscillator Configuration: The dsPIC33FJ16GS504 microcontroller's oscillator system provides options for both internal and external oscillator clock sources, clock switching between clock sources, and a monitor that detects clock failure and takes certain failsafe measures. Figure 2.21 shows the oscillator system.

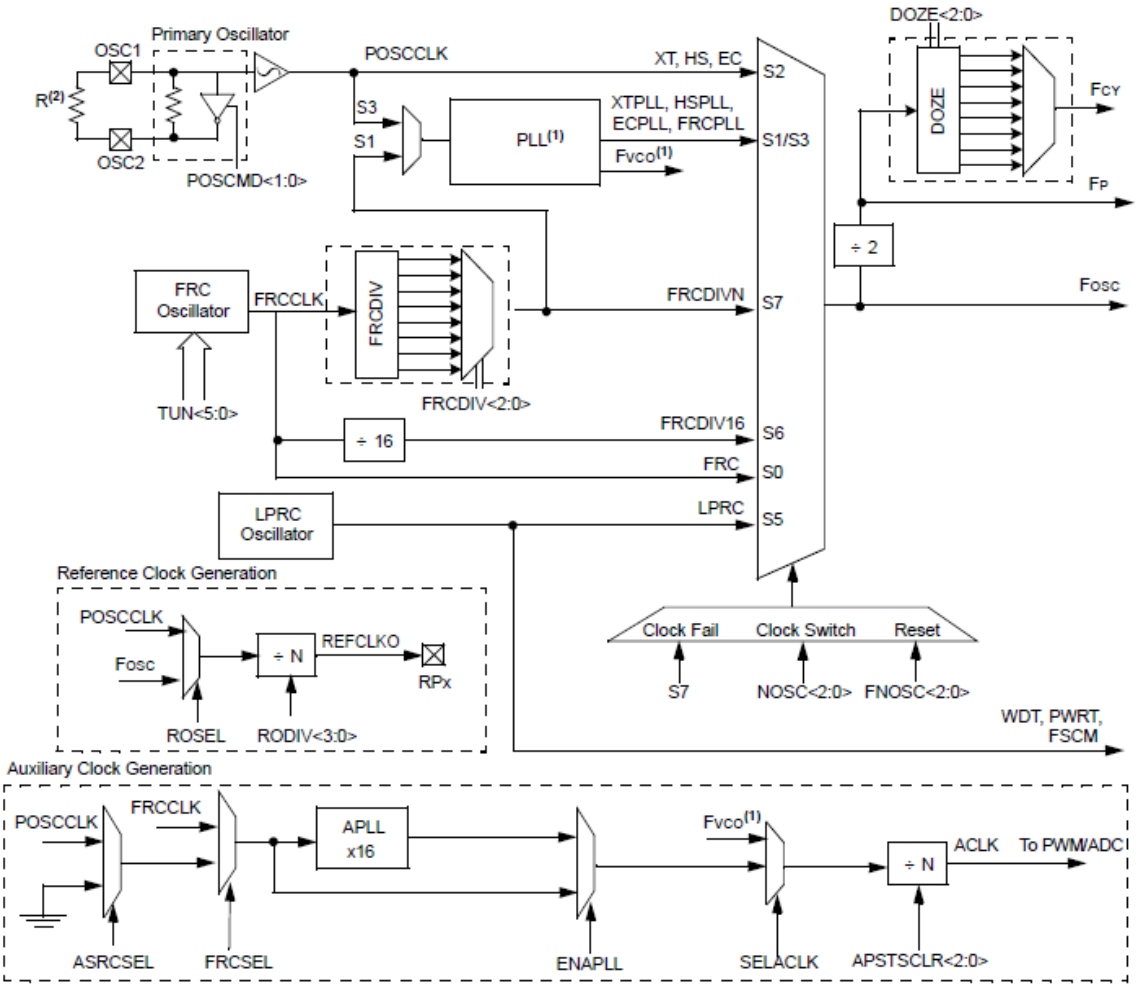


Figure 2.21 - Oscillator System for the dsPIC33FJ16GS504 PIC Microcontroller (Permission requested from Microchip)

Six clock options are available, including fast RC oscillator, FRC oscillator with PLL, primary oscillator, primary oscillator with PLL, low power RC oscillator, and FRC oscillator with postscaler. The primary oscillator may consist of (XT) crystal and ceramic resonators from 3 MHz to 10 MHz, (HS) high-speed crystals from 10 MHz to 40 MHz, or (EC) an external clock signal applied to the OSC1 pin. The low power RC oscillator runs at 32.768 kHz and is utilized by the Watchdog

Timer and Fail-Safe Clock Monitor. There are a total of twelve possible clock modes, outlined in Table 2.13.

Oscillator Mode	Oscillator Source	POSCMD <1:0>	FNOSC <2:0>
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110
Low-Power RC Oscillator (LPRC)	Internal	xx	101
Reserved	Reserved	xx	100
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011
Primary Oscillator (HS)	Primary	10	010
Primary Oscillator (XT)	Primary	01	010
Primary Oscillator (EC)	Primary	00	010
Fast RC Oscillator with PLL (FRCPLL)	Internal	xx	001
Fast RC Oscillator (FRC)	Internal	xx	000

Table 2.13 - Oscillator Clock Modes for the dsPIC33FJ16GS504 PIC Microcontroller (Permission requested from Microchip)

The PLL can be used by the primary oscillator and the internal FRC oscillator to reach increased operation speeds. The output of the primary or FRC oscillator is designated F_{IN}. Figure 2.22 shows the PLL block diagram.

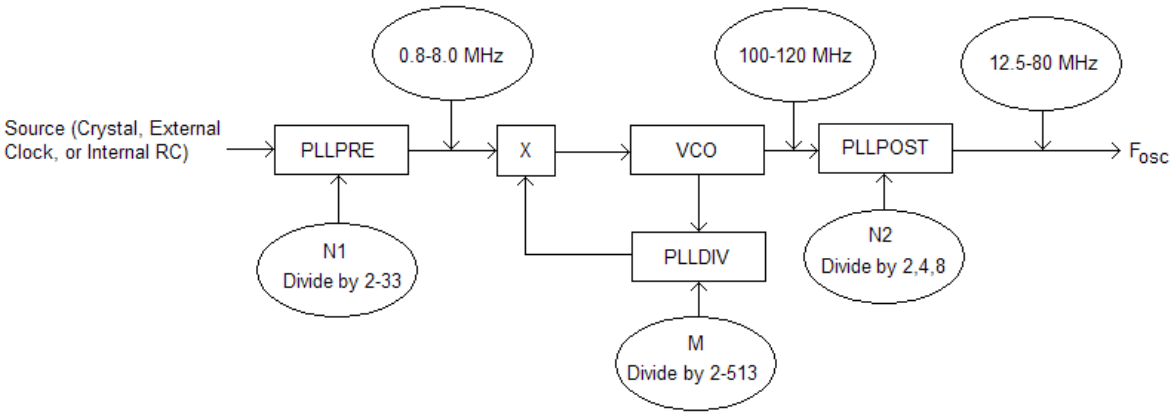


Figure 2.22 - PLL Block Diagram for the dsPIC33FJ16GS504 PIC Microcontroller

The factors N1, M, and N2 are used to control the frequency, maintaining a specified range. The output of the PLL, designated F_{OSC}, is given by the equation:

$$F_{OSC} = F_{IN} \times (\frac{M}{N1 \times N2})$$

The device operating frequency is given by:

$$F_{CY} = \frac{F_{OSC}}{2}$$

2.2.6 Op-Amps

Op-amps, or operational amplifiers, are high-gain voltage amplifiers. Figure 2.23 shows the internal circuitry that is contained in a typical op-amp. This circuitry is defined by three stages. The first, a differential amplifier, provides high input impedance and low noise amplification. The second, a voltage amplifier, provides high voltage gain. The third, an output amplifier, provides high current driving capability and low output impedance [11].

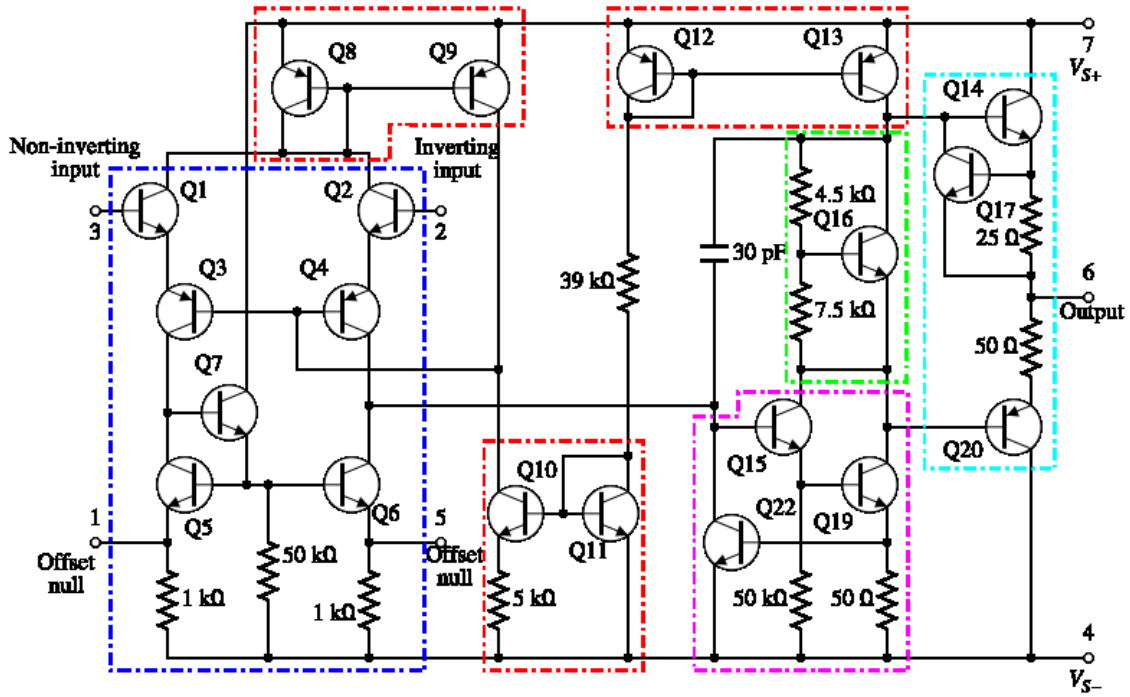


Figure 2.23 - Operational Amplifier Internal Circuitry.
Reprinted under terms of license [12]

This circuit diagram identifies the current mirrors, outlined in red; the differential amplifier, outlined in blue; the class A gain stage, outlined in magenta; the voltage level shifter outlined in green; and the output stage, outlined in cyan.

2.2.7 Power Factor Correction

The power factor is given by a ratio of the real power to the apparent power. The value of the power factor can range from 0 to 1, and this value can result in significant harmonic distortion. If the load is pure resistance, the power factor will be equal to 1 and no harmonic distortion will occur. If the load is less than 1, harmonic distortion will occur. A power factor of 0.999 corresponds to 3% harmonic distortion, while a power factor of 0.95 corresponds to 30% harmonic distortion [13]. Clearly, the highest power factor possible is desirable.

A boost regulator has advantages for active power factor correction because of its continuous input current, which minimizes noise conducted and produces the optimal input current waveform. However, it requires high output voltage. The VIENNA rectifier is able to convert variable amplitude and variable frequency voltage to a DC voltage, and also controls the input current, producing a sinusoid in phase with the input voltage. Thus, the VIENNA rectifier is sufficient for power factor correction with a power factor very close to one.

2.2.8 Global Positioning System

The wave generator and power management circuit will be placed on a buoy in the middle of the ocean. The buoy will be tethered to the underwater components. However, if the tether were to break, the buoy will float off aimlessly in the ocean. So, the power management circuit will be outfitted with a Global Positioning System (GPS) module to determine if the buoy becomes disconnected from its tether. If so, the GPS will help engineers locate the wandering buoy. There are many GPS units to choose from. A GPS module that uses a standard protocol and can be easily interfaced to a microcontroller is a must. Currently, the standard protocol for GPS units is the NMEA 0183 protocol. A NMEA 0183 message begins with $GP and ends with a carriage return. Data elements are separated by commas and terminated by the * character. Each message ends with the checksum and hex value of the calculated checksum. A GPS module will immediately begin acquiring satellites after power is supplied. After it acquires at least 3 satellites, it will begin reporting its position. The satellite tracking status is reported by the module using two commands. The GSA command includes a field that indicates whether or not there are enough satellites to get a signal. To obtain positional data, two other commands must be used. These commands are GGA and RMC. The GGA command provides you with the time, position and fixes type. The RMC command provides you with the time, date, position, course and speed. To receive all the necessary information, both commands must be used. The longitude and latitude can be obtained from

either, but only GGA will report the altitude and fix type. The RMC command will be used to obtain the course and speed. The command formats are listed in detail below:

GGA: Global Positioning System Fixed Data

Field 1, UTC Time in the format of hhmmss.sss
Field 2, Latitude in the format of ddmm.mmmm
Fields 3, N/S Indicator (N=North, S=South)
Field 4, Longitude in the format of dddmm.mmmm
Field 5, E/W Indicator (E=East, W=West)
Field 6, Position Fix Indicator (0=No Fix, 1=SPS Fix, 2=DGPS Fix)
Field 7, Satellites Used (0-12)
Field 8, Horizontal Dilution of Precision
Field 9, MSL Altitude
Field 10, MSL Units (M=Meters)
Field 11, Geoid Separation
Field 12, Geoid Units (M=Meters)
Field 13, Age of Diff Correction in seconds
Field 14, Diff Reference

RMC: Recommended Minimum Specific GNSS Data

Field 1, UTC Time in the format of hhmmss.sss
Field 2, Status (A=Valid Data, B=Invalid Data)
Field 3, Latitude in the format of ddmm.mmmm
Fields 4, N/S Indicator (N=North, S=South)
Field 5, Longitude in the format of dddmm.mmmm
Field 6, E/W Indicator (E=East, W=West)
Field 7, Speed over ground in knots
Field 8, Course over ground in degrees
Field 9, Date in the format of ddmmyy
Field 10, Magnetic Variation in degrees
Field 11, Mode (A=Autonomous, D=DGPS, E=DR)

The EM-406A, EM-408, Etek, Copernicus and Holux GPSSlim 236 modules all support the NMEA 0183 protocol and can interfaced to a microcontroller. The EM-406A is manufactured by USGlobalSat. It has an optional development board that well suited for interfacing to a PC. The EM-406A can be seen in Figure 2.24.

EM-406A Specifications:

- 20 Channel Receiver
- Built-in antenna
- High sensitivity: -159dBm
- 30’ Positional Accuracy / 25’ with WAAS

- Supports WAAS in default mode.
- Hot Start : 8 seconds
- Warm Start : 38 seconds
- Cold Start : 42 seconds
- 70mA power consumption
- 4.5 – 6.5 volt operation
- Outputs NMEA 0183 and SiRF binary protocols
- Small foot print : 30mm x 30mm x 10.5mm
- Built-in LED status indicator
- 6-pin interface cable included

Figure 2.24 - EM-406A GPS Receiver
(Permission requested from Sparkfun)

The EM-408 module shown in Figure 2.25 is also manufactured by USGlobalSat. This module doesn't have its own evaluation board. It does have a built-in antenna and a MMCX connector for attaching an external antenna. Both the EM-406A and the EM-408 outputs its data at 4800 baud, 8N1.

EM-408 Specifications:

- 20 Channel Receiver
- Built-in antenna
- High sensitivity: -159dBm
- 30' Positional Accuracy / 25' with WAAS
- Supports WAAS in default mode.
- Hot Start : 8 seconds
- Warm Start : 38 seconds
- Cold Start : 42 seconds
- 75mA power consumption
- 3.3 volt operation
- Outputs NMEA 0183 and SiRF binary protocols

- 30gram weight
- Built-in LED status indicator
- 5-pin interface cable included
- External MMCX antenna connector

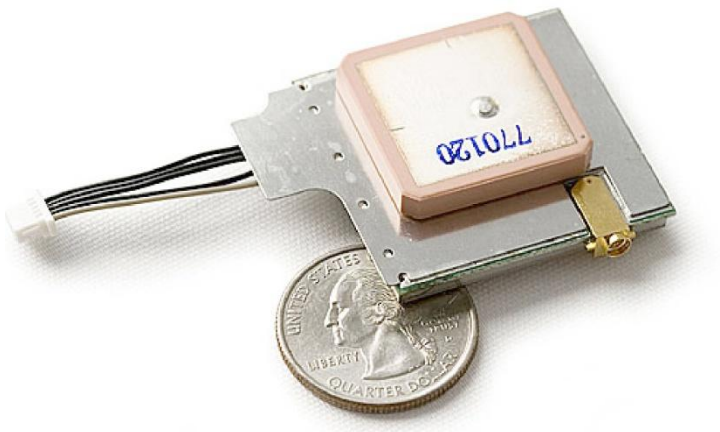


Figure 2.25 - EM-408 GPS Receiver
(Permission requested from Sparkfun)

NAVIBE 611 Sport GPS

The NAVIBE 611 shown in Figure 2.26 is a small GPS module that operates off 2 AA Batteries. It can also be powered via the rear connector. It features a small connector that provides both a serial and USB interface. It also has data logging capabilities.

NAVIBE 611 Sport GPS Specifications:

•Durable orange rubberized housing
•12 parallel channels for fast acquisition and reacquisition
•Supports standard NMEA 0183 protocol
•Water resistant housing
•LCD display shows distance, average/max speed
•Operates on two (2) AAA batteries
•Can also be used as a USB GPS receiver

Figure 2.26 - NAVIBE 611 Sport GPS Module
(Permission requested from Navibe)

The Holux GPSlim236 shown in Figure 2.27 supports a Bluetooth wireless interface and has a built-in battery that will power the module for 10 hours. The connector is a noninverting TTL serial interface that can be used when interfacing with a microcontroller.

Holux GPSlim236 Specifications:

• Dual function (Bluetooth GPS+ G-mouse)
•20 parallel satellite-tracking channels for fast acquisition and reacquisition
• Compatible with Bluetooth Serial Port Profile (SPP) completely
• Built-in rechargeable Lithium ion battery without external power supply for at least 10 hours operation.
• Built-in 850mAh rechargeable battery for memory and RTC backup and for fast Time To First Fix (TTFF).
• Support NMEA0183 v2.2 data protocol or SiRF binary code
• FLASH based program memory
• New software revisions upgradeable through serial interface

Figure 2.27 - Holux GPSlim236 Module
(Permission requested from Holux)

2.3 Software Research

As mentioned previously, the software used in this project will be limited to PC software and controller software. In today's fast emerging market, there are various options and hence it was necessary to research them in detail. Under PC software, there are few important components that need to be researched:

2.3.1 User Interface

It was established that the user interface will need to be a powerful graphical user interface (GUI) application for debugging and logging data purposes. While the user interface will not have any impact on the functional performance of the project, it will provide several particularly useful features. These include the observation of the completed converter's operation; the logging of data for retrieval at a later time; and the display of system operation for the purposes of debugging as the converter is being perfected.

Furthermore, the GUI will provide capability for the software to be updated in the field. This will allow for modification as deemed necessary in the future, or for the correction of potential errors that may be discovered.

2.3.2 PC Communication

One of the ways to establish long communication between the PC and digital controllers is via a serial. Although, the serial connection requires a large voltage swing i.e. ± 12V, it still is one of the easiest way to transfer data. A serial connection only requires three wires – receive, transmit, and ground.

Another method of communication could be though a Wi-Fi port. A Wi-ranger is already in place inside the DAQ box of the sensor package. It should not be too difficult to integrate

2.3.3 Power Factor Correction (PFC)

As known, the power will be generated from a generator. Hence, this power will be of non-linear nature and it will be important to maintain a regular flow of power. In order to do the same, a Power Factor Convertor (PFC) will be placed in the design. There are two kinds of Power Factor Correctors: Passive PFC and Active PFC.

For this design, it was determined that a passive PFC will be undesirable as it requires large and expensive inductors. Also, they are known to be less efficient in correcting the load nonlinearity.

An Active PFC will be used to control the amount of power drawn by the load and obtain a power factor close to unity.

2.3.4 GPS

A GPS software will be built that will basically consist of an interface. This interface will contain data acquired from the GPS unit as well as it will display alarms in case the buoy has been dislocated from its radius.

2.3.5 Digital Controller

The control system controllers can be classified in four main types:

1. Proportional Controllers (P Controllers) – These controllers are simple controllers that are used to provide stable gain. Supplying a proportional gain is one of the main features of such controller. This is achieved by overshoot compensation and ripple voltage minimization. The proportional gain achieved by such systems is fairly low. Hence, P Controllers alone are not a desired option for control systems requiring high proportional gain.
2. Proportional-Derivative Controllers (PD Controllers) – These controllers basically are used to compensate for some future error value. For highly varying output systems, such controllers are desired as they provide a proportional derivative gain. Although such systems greatly reduce overshoot and ripple, they are inefficient as a small amount of high frequency noise can have a large distortion in the system. Hence, it is possible for the PD Controllers to set a value that is far from the desired output value.
3. Proportional-Integral Controllers (PI Controllers) – Opposing to the PD Controllers, the PI Controllers are used to compensate for some past value errors. By taking an integral of the output value minus the desired value, this controller compensates for the steady-state error by minimizing it to zero, unlike the P Controller. Also, unlike the PD Controller, the PI Controller maintains a steady signal in case of high frequency noise due to the lack of derivative action. However, such controllers are much slower and less responsive and hence undesirable for the project.
4. Proportional-Integral-Derivative Controller (PID Controller) – A PID Controller is a combination of all three – Proportional, Integral and Derivative Controller. This controller takes a proportional constant and adds it to the current output. Then, the error generated from it will be integrated and added on to the system which makes the system steady-

state. Finally, the derivative action is provided in order to control the output for any change or disturbance. Such controllers are flexible and can be programmed to achieve desirable outputs with high accuracy. Hence, a PID Controller is the most suited option for the project.

A proportional-integral-derivative (PID) controller will be used as a feedback controller. A simple algorithm will be created for controlling the different voltages and currents. Figure 2.28 depicts a block diagram image of a PID controller.

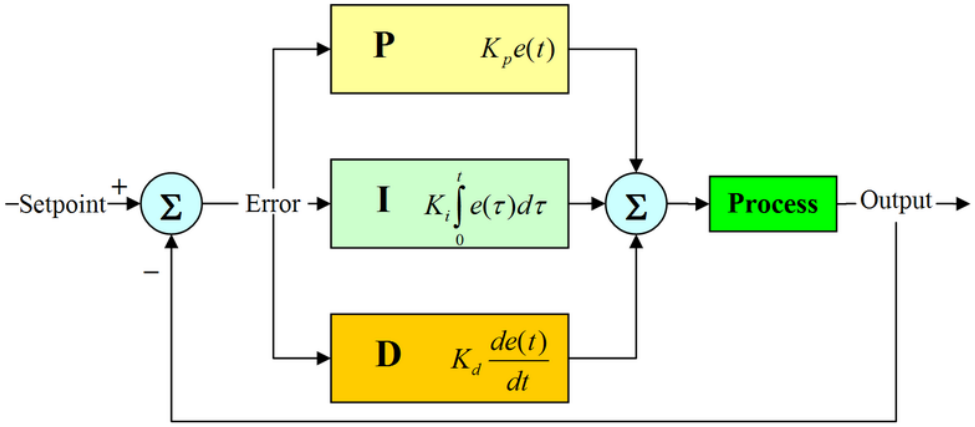


Figure 2.28 - Block Diagram of a PID Controller (Reprinted under CC-BY-2.5; Released under the GNU Free Documentation License)

2.3.6 PIC Microcontroller

In order to efficiently program the dsPIC microcontrollers, a software program must be chosen that can provide professional results and be easy to troubleshoot. A suitable compiler will not only determine the productivity of the microcontroller but also overall efficiency of the system. The software packages will be examined by looking at its programming language, availability of GUI and the built-in libraries. Cost of the software will also be a factor in determining the most appropriate software package.

After rigorous research, the options were narrowed down to MicroChip's MPLAB, MikroC Pro by MikroElektronica and HI-Tech owned by MicroChip which are reviewed below

MikroC Pro – MikroC Pro is a product of MikroElektronica. This product has applications to a wide variety of dsPIC microcontrollers, just short of 250 different families including dsPIC 12/16/18/24/30/33. The company also offers products with different programming languages such as MikroBasic and MikroPascal that offers the programmer to program in Basic and Pascal environments respectively. However, it was predetermined to program in C language and hence MikroC was the best choice out of the other products. This software package introduces new and innovative ways of programing the microcontroller.

These features include a powerful compiler, extended in-built libraries including hardware interfacing and DSP libraries, an IDE with various environments including a preview window in flash screen, a software simulator, and a powerful In-Circuit Debugger (ICD) called MikroICD which allows the user execute real-time programs to debug code. MikroElektronica encourages consumers to purchase their hardware along with the software utility package in order to receive a discounted price. The price of the software package alone is $249.99. They also provide a free trial version that could be used except there is a code limit on it.

MPLAB — Microchip supplies three editions of MPLAB C compilers for dsPIC33F DSC line of microcontrollers. Each are ANSI x3. 159-1989-compliant Windows applications that serve as a platform for the development of C code. The compiler also includes a command-line driver program that enables application programs to be compiled, assembled, and linked with one step. The Standard compiler must be purchased, and it features all optimization levels. The free Standard Evaluation compiler features all optimization levels for 60 days before downgrading to level one optimization. The free Lite compiler offers only optimization level one. While higher optimization levels could reduce the amount of code or increase the speed to an extent, the dsPIC33FJ12GS504 microcontroller has a significant amount of flash memory and should not suffer for a low optimization level. Considering that the MPLAB compiler is free, and that it is offered by Microchip specifically for use with their microcontrollers, it seems the most logical choice for this project.

HI-TECH – (now owned by Microchip) offers a freestanding, optimizing ANSIC compiler that supports PIC and dsPIC devices. The compiler is available for all popular operating systems both 32-bit and 64-bit. As well as being a stand-alone console application, it is fully compatible with Microchip's MPLAB IDE. This allows a user to develop in MPLAB and compile with HI-TECH. The compiler includes many built in functions and it produces highly efficient machine code. The retail cost of this complier places it outside of the budget of this project. However, they do offer a LITE version of the complier for free at htsoft.com. The compiler also integrates into HI-TIDE. This is an IDE based on Eclipse. The HI-TECH compiler produces small, tight, fast code. However, it isn't as user-friendly as its MikroC and MPLAB counterparts are.

Chapter 3: Design

3.1 Hardware

Figure 3.1 depicts the complete block diagram for the entire hardware circuit. According to the different blocks, this section has been broken down into appropriate sections.

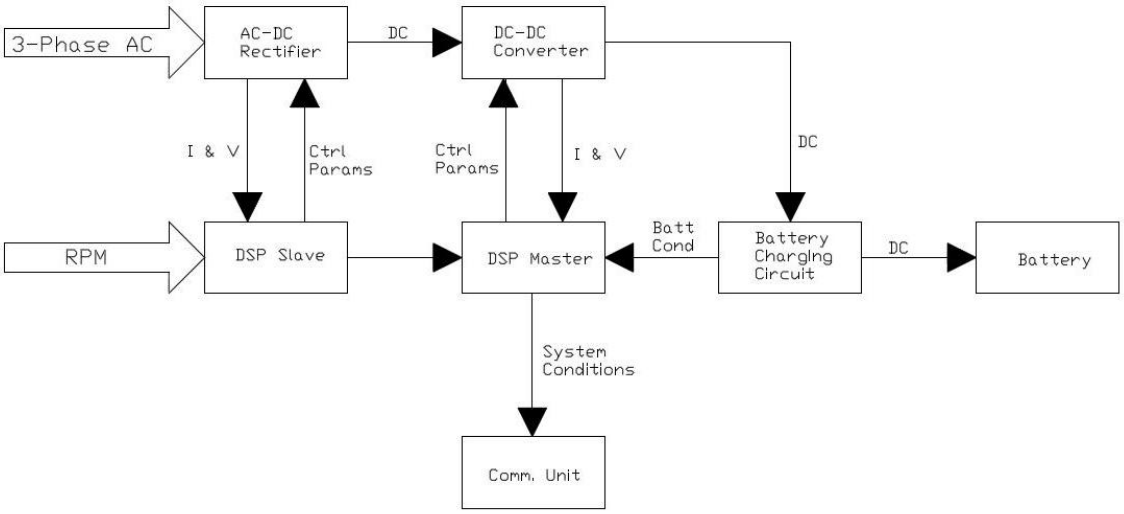


Figure 3.1 - Complete Block Diagram of Power Management Circuit

3.1.1 AC/DC Rectifier with Boost Converter

The mechanical engineering team will design a turbine to drive a Ginlong permanent magnet generator. This generator will produce a 3-phase output of variable frequency, current, and voltage. This output will be rectified to a constant DC voltage. That DC voltage will be stepped down to 12volts. The 12volt output will be used to charge a battery and power the internal circuitry. Both the rectifier and converter will be realized with digital control mechanisms. In particular, two DSP microcontrollers will run simple control algorithms to monitor and adjust the rectifier and converter. The latter should help elucidate how the system operates as a whole. The arrows indicate signal flow and direction. Lastly, signals within the blocks are digital and signals between the blocks are analog.

There are many designs for accomplishing AC to DC rectification. In a low cost, low power environment, a designer could use a simple diode bridge rectifier and capacitor voltage filter. However, as the power requirements increase, this design becomes more inefficient and places high stress on the components. Thus, for high power applications, a three-phase input helps lower the stress on components and reduce component size. A controlled three-phase rectifier can be isolated or non-isolated. The AC-DC rectifier in this design will be non-isolated

because isolation will be achieved in the DC-DC converter. The rectifier will be the interface between a variable speed generator and a constant DC bus. High efficiency conversion can be realized if a power factor close to 1 is achieved at the source input. Research was also narrowed to unidirectional converters because the conversion will only occur in one direction for this application. Lastly, a boost topology will be required because the three-phase input will correspond with the rotational speed. Three rectifiers were compared and the VIENNA rectifier was finally chosen.

VIENNA Input Conductor Design — Inductor analysis was accomplished by first obtaining a plant control model of the VIENNA rectifier. See Figure 3.2.

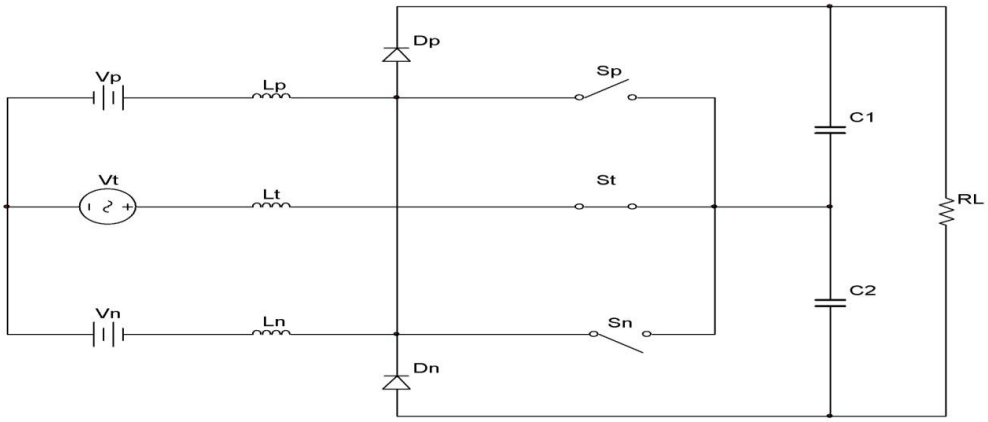


Figure 3.2 - Plant Control Model of VIENNA Rectifier

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Assuming $D_p > D_n$, the positive inductor L_p is charged during the period $(D_p T_{sw})$ and discharged during the period $[(1 - D_p)T_{sw}]$. The current waveform of L_p during the period T_{sw} is shown in Figure 3.3.

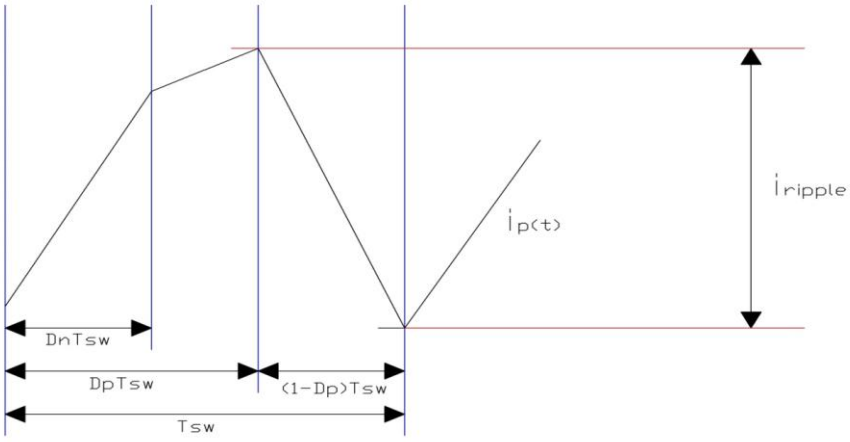


Figure 3.3 - Positive Side Current Waveform when Dp > Dn

Assuming large capacitors are used and the voltage ripple is minimized, the current waveform during the off cycle can mathematically be derived as:

$$i_p(t) = i_{p0} + \frac{1}{L}\int_{D_pT_{sw}}^{T_{sw}} V_{diff}\,dt$$
$$= i_{p0} + \frac{1}{L}\int_{D_pT_{sw}}^{T_{sw}} -\big(V_p(t) - E\big)dt$$
$$= i_{p0} - \frac{\big(V_p(t)-E\big)\big(1-D_p\big)T_{sw}}{L}$$

Note: i_{p0}= initial current & V_{diff}= voltage over inductor

The current ripple is equivalent to the current waveform with an adjusted time period such that:

$$i_{ripple}(t) = -\frac{\big(V_p(t)-E\big)\big(1-D_p\big)T_{sw}}{L_p}$$

The positive and negative rail voltages can be represented mathematically as:

$V_p = V_{phase,peak}\cos\left(k\omega t - \frac{\pi}{3}\right)$ for $(0 \leq \boldsymbol{\omega t} < \frac{\boldsymbol{\pi}}{\boldsymbol{3}})$
$V_n = -V_{phase,peak}\cos(n\omega t + 0)$ for $(-\frac{\pi}{3} \leq \boldsymbol{\omega t} < \frac{\boldsymbol{\pi}}{\boldsymbol{3}})$

The maximum current ripple occurs when $\boldsymbol{\omega}t = \frac{\pi}{6}$. Thus, $V_p = 0.866V_{phase,peak}$ & $V_n = -0.866V_{phase,peak}$ Substituting the latter into the $i_{ripple}(t)$ equation yields the maximum current ripple:

$$i_{ripple,max} = -\frac{0.866V_{phase,peak}}{E}\frac{\big(0.866V_{phase,peak} - E\big)T_{sw}}{L}$$

The goal is to find the input inductance required for a particular amount of current ripple at 86.6% of the peak voltage. This can be accomplished by rearranging the equation above to obtain:

$$L = -\frac{0.866V_{phase,peak}}{E}\frac{\big(0.866V_{phase,peak} - E\big)T_{sw}}{i_{ripple,max}}$$

VIENNA Output Capacitor Design — Inductor analysis was accomplished by first obtaining a plant control model of the VIENNA rectifier. See Figure 3.2.

reference to the figure above, the current ripple is Assuming $D_p > D_n$, the positive inductor L_p is charged during the period $\big(D_pT_{sw}\big)$ and discharged during the period $\big[\big(1 - D_p\big)T_{sw}\big]$. The current waveform of L_p during the period T_{sw} is shown in Figure 3.3.

VIENNA Power Stage Design — The generator can produce an open circuit voltage of 40V (line-to-line) at 220 rpm. At this rpm, the generator can supply 220 watts. Thus, the VIENNA must be able to supply 400W of output power at 80V (line-to-line) of input voltage. The peak phase voltage can be calculated as:

$$V_{phase,peak} = \sqrt{2}\left(\frac{V_{LL,max,rms}}{\sqrt{3}}\right) = \sqrt{2}\left(\frac{40V}{\sqrt{3}}\right) = 32.66\ V$$

The output voltage can be calculated as:

$$V_{out} = \left(3V_{phase,peak}\right) = (3 * 32.66\ V) = 97.97\ V$$

Assuming the voltage over the first capacitor is equal to the voltage over the second capacitor, where E = V_1=V_2, E can be calculated as:

$$E = \frac{V_{out}}{2} = \frac{97.97\ V}{2} = 48.99\ V$$

The rms phase input current is equal to:

$$i_{phase,rms} = \frac{P_{out}}{3\left(\frac{V_{LL}}{\sqrt{3}}\right)} = \frac{150\ W}{3\left(\frac{40\ V}{\sqrt{3}}\right)} = \frac{150\ W}{69.28\ V} = 2.17\ A$$

The peak average phase input current is equal to:

$$i_{phase,peak} = \sqrt{2} i_{phase,rms} = \sqrt{2} * 2.17A = 3.06\ A$$

The switching frequency f_{sw} was arbitrarily chosen to be 50 kHz. Then, the period of one switching cycle can be calculated as:

$$T_{sw} = \frac{1}{f_{sw}} = \frac{1}{50kHz} = 20\mu s$$

The values above can be substituted into the inductor equation to yield an approximate value of 47 µH. The maximum output current of the rectifier is simply the power out divided by the output voltage.

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{150\ W}{97.97\ V} = 1.53\ A$$

Determining the output capacitance of the VIENNA rectifier is more complicated. Thus, rather than performing rigorous calculations or writing lengthy Matlab code, the value was approximated by researching other VIENNA circuits that had similar characteristics. A reasonable value for this circuit is $\approx 22\mu f$. Since both the positive and negative duty cycles are symmetric, either D_p or D_n can be set equal to 1 for plant analysis. The control of this rectifier will be accomplished digitally. Thus, a reference voltage was chosen to be equal to half of the operating voltage of the processor. The dsPIC33F family of 16-bit

microcontrollers has been chosen for system control. These controllers generally have a voltage range of 3.0 V - 3.6 V. Therefore, setting the operating voltage to 3.3V yields: V_{ref} = $\frac{3.3V}{2}$ = 1.65V. This will allow for adequate output swing to both rails.

VIENNA Digital Controller Design — Originally, an analog compensator for the rectifier was considered: See Figure 3.4. The transfer function for the compensator was obtained as:

$$T_c(s) = 11492\frac{(s+291.5)}{s(s+3430.8)}$$

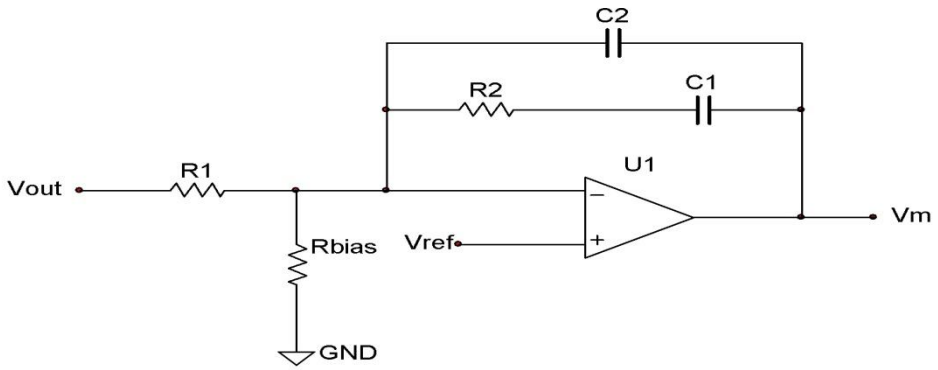


Figure 3.4 - Analog Type II Compensator Implemented with Operational Amplifier

However, after considering the benefits of using a DSP and running a simple control algorithm. It was decided to convert the analog compensator to its digital equivalent. The Z-transform equivalent of the transfer function is given by:

$$T_c(z) = (1-z^{-1})Z\left\{\frac{T_c(s)}{s}\right\} = \frac{z-1}{z}Z\left\{\frac{A_G(s+\omega z)}{s^2(s+\omega p)}\right\} = \left[\frac{a_1+z^{-1}a_2+z^{-2}a_3}{b_1+z^{-1}b_2+z^{-2}b_3}\right]$$

The controller coefficients are listed in the Table 3.1:

a_1=	$A_G(A+C) \approx 0$
a_2=	$A_G(A(-1-e^{-\omega pT}) + BT - 2C)$
a_3=	$A_g(Ae^{-\omega pT} - BTe^{-\omega pT} + C)$
b_1=	1
b_2=	$(-1-e^{-\omega pT})$
b_3=	$(e^{-\omega pT})$

where

A=	$\frac{\left((1+\omega_z) - B(1+\omega_p) - C\right)}{(1+\omega_p)}$
B=	$\frac{\omega_z}{\omega_p}$
C=	$\frac{-(\omega_z - \omega_p)}{{\omega_p}^2}$

Table 3.1 - Controller coefficients for Digital Signal Processor

The flow diagram in Figure 3.5 provides a graphical representation of the transfer function.

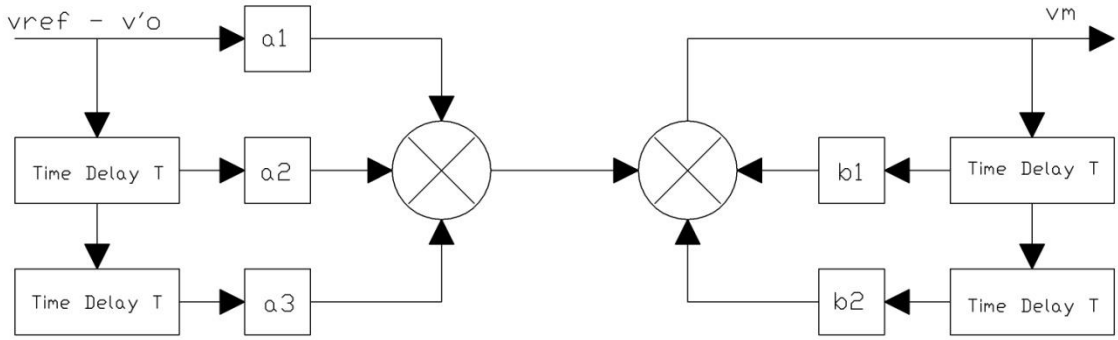


Figure 3.5 - Digital Lag-Lead Compensator Flow Diagram

If the sampling frequency is kept sufficiently high, its performance will remain comparable to its analog counterpart.

Digital Implementation of a Low Pass Filter — The sensed input current control signals must be filtered in order to reject high frequency switching noise and thus obtain proper closed-loop system operation. For this implementation, a low pass filter with a DC gain of 1 and a -3dB cut-off frequency an order magnitude higher than the cross-over frequency is required. A DC unity gain is preferred so that the gain response of the system remains the same. Choosing a cut-off frequency an order of magnitude higher than the crossover frequency ensures that the phase profile of the system will not change. The cut-off frequency must be chosen in this fashion because the filter phase is still in transition up to an order of magnitude below the cut-off frequency. The transfer model of the filter is given in Laplace form as:

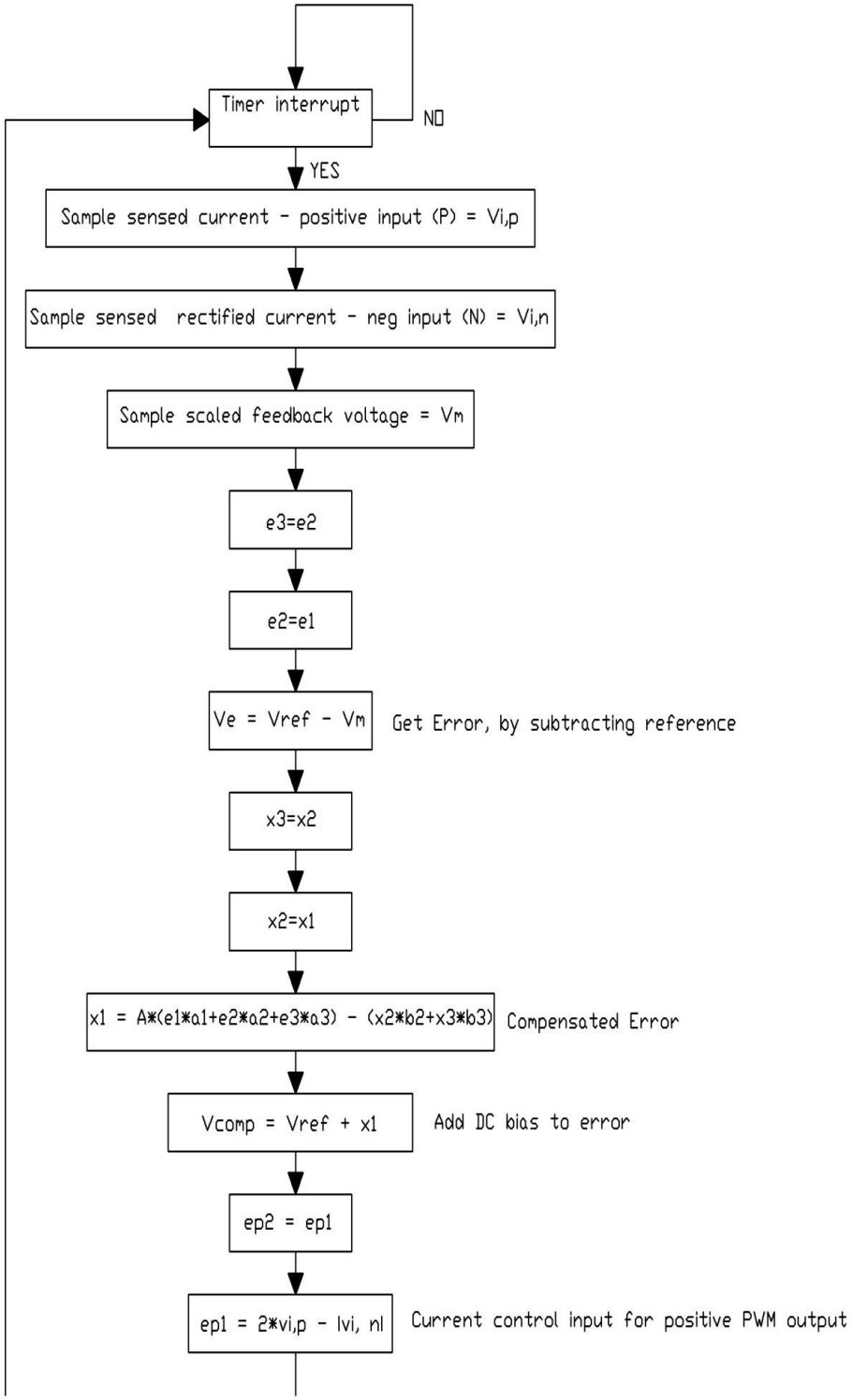
$$T_{filter}(s) = \frac{1}{\frac{s}{\omega filter} + 1}$$

The equivalent z-transform is:

$$T_{filter}(z) = \frac{z\omega filter}{z - e^{-\omega filterT}} = \frac{z^{-1}\left(1 - e^{-\omega filterT}\right)}{1 - z^{-1}e^{-\omega filterT}}$$

Digital Controller Implementation — The foundation of this circuit lies in digital controls. The first stage in the load management circuit is rectification. The VIENNA rectifier will be controlled digitally via a DSP chip running two major control algorithms. The first algorithm will perform power factor correction by sampling the voltage and current of the 3-phase input. Based on these samples, the switching duty cycle will be varied in an effort to keep the input power at its

maximum by ensuring the current and voltage are in phase. The algorithm can be best explained by examining the flow diagram in Figure 3.6.



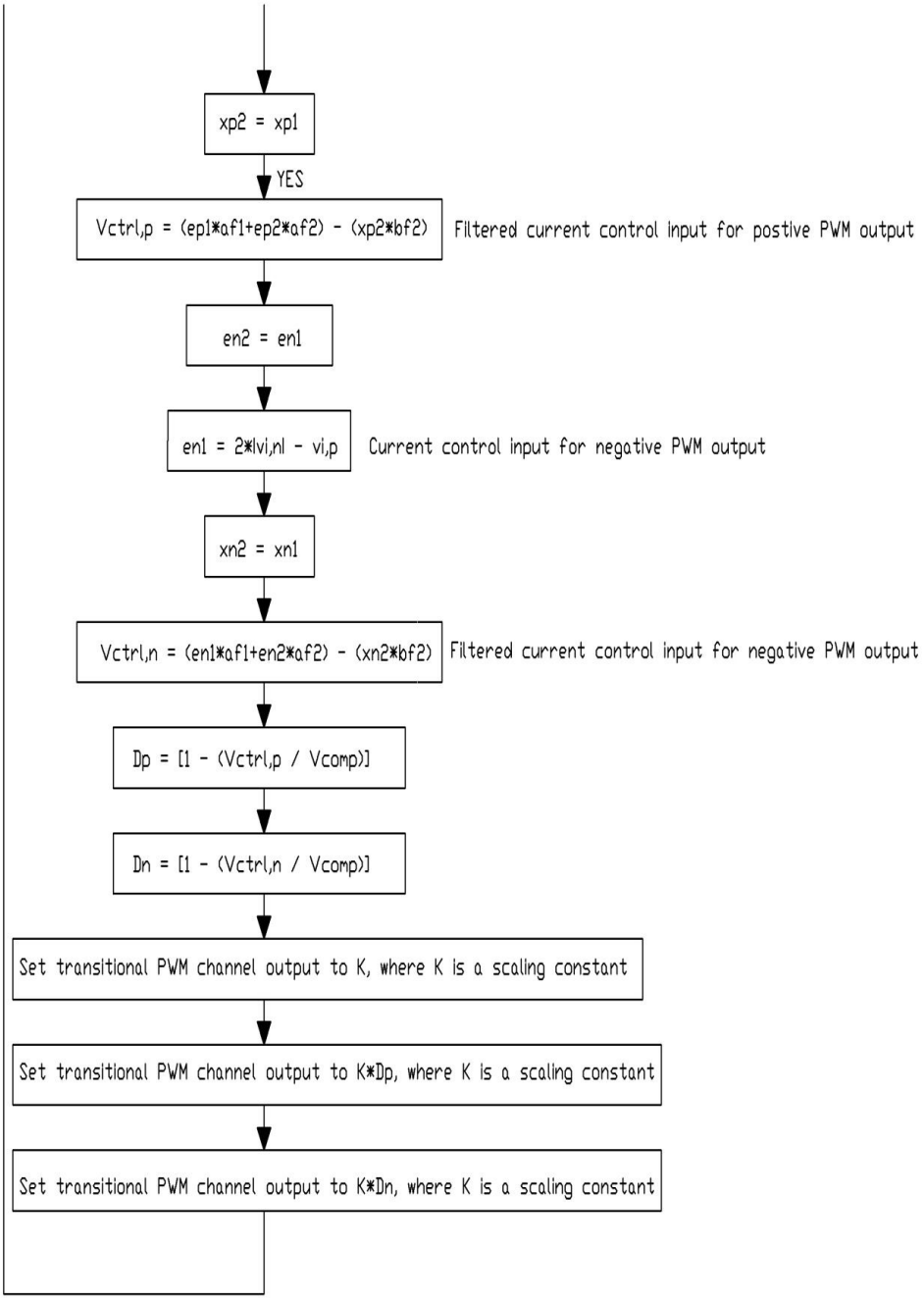


Figure 3.6 - Flow Diagram of PFC digital controller

The generator won't always be producing the same output. In fact, because the generator relies on deep water oceans waves, the output will vary significantly. Thus, a control algorithm is required to present an optimal electrical load to the generator at all times. The algorithm will perform maximum power point tracking. Several MPPT algorithms currently exist. The most popular is perturb and observe (PO). This method basically alters the current or voltage by a fixed amount in a given direction repeatedly until it detects a drop in power between

the changes. If a drop in power is noticed, the current or voltage will be altered by a fixed amount in the opposite direction. The system never actually reaches a maximum power point. Instead, it oscillates about the MPP. Also, even though this algorithm benefits from simplicity, it lacks the speed and adaptability to track fast transients.

Instead of searching for the PV voltage or current that result in max MPP, a new algorithm will be developed to directly track the maximum possible power. It works be first setting the maximum power P_{max} to an initial value, say zero. The instantaneous value of PV is computed and stored as P_{act}. The error between P_{max} and P_{act} is used as the input to an ON/OFF controller with hysteresis band. The error between P_{max} and P_{act} is checked to track maximum power. If the error is below the 0.5 W upper limit, the power drawn from PV is reasonable and P_{max} can be incremented. The new value of P_{max} is stored and used to track PV on the next iteration. The algorithm is repeated and the computed value of P_{max} will steadily increase and the power extracted will be matched to this computed value as long as the actual power P_{act} is within the tolerance band of hysteresis controller. Otherwise, the value of P_{max} must be reduced because it is greater than the maximum possible PV. The reduction will repeat until the error between P_{max} and P_{act} is minimized. The algorithm can be most easily explained by examining Figure 3.7.

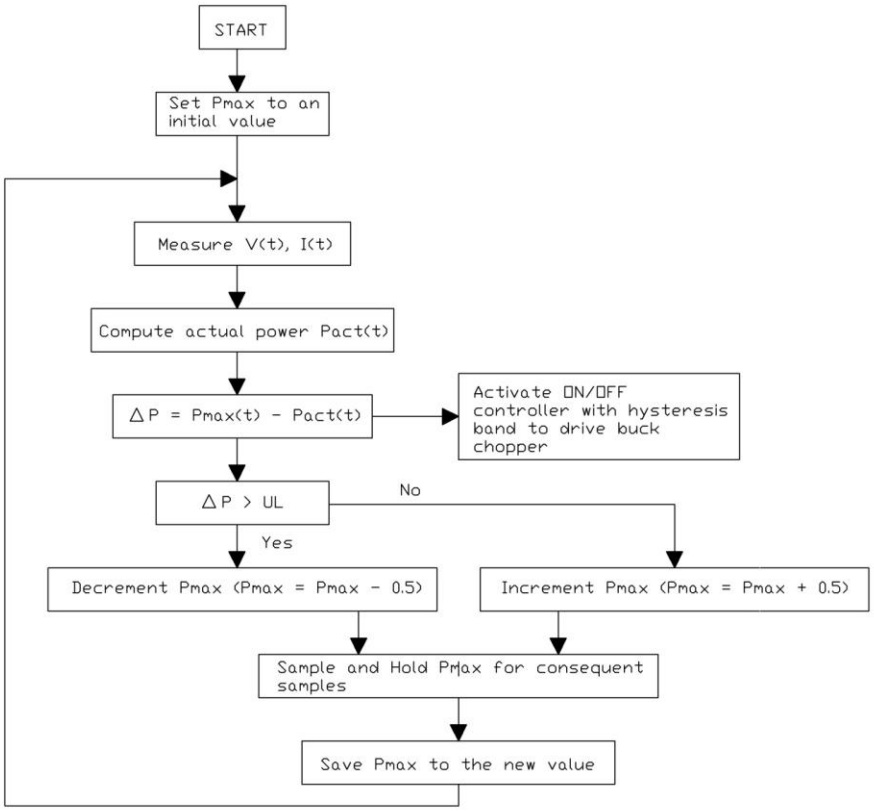


Figure 3.7 - Flowchart of Proposed MPPT Algorithm

The slave DSP will also actively monitor and report several parameters to the master DSP. The latter includes the input and output power, duty cycle, power factor, and present efficiency. The second stage of the system is a high efficiency step down DC-to-DC converter. The output voltage will be regulated to 12 volts for charging a battery. The master DSP will operate proportional integral controllers that control the voltage (input and output) and the current output. The control software for this stage is run on the master DSP. Basically, the duty cycle of MOSFET switch is varied in order to achieve desired values. Additionally, the master controller will also monitor the battery's charge and temperature. It will also monitor short circuits. Periodically, an operator may wish to connect an external computer to the system to gather data and monitor efficiency. Also, the ability to connect an external computer and alter/add code to the system is highly desirable. System parameters may change (adding a new generator, different battery etc) and having this ability will greatly increase the flexibility/adaptability of the design. Thus, the master DSP will optionally interface with an external computer. The computer can be used to gather data for performance analysis or debugging purposes. It can also be used add code, execute new instructions or alter the control algorithms. Finally, the external PC software is an optional component to the system, not required for the system to run.

3.1.2 DC-DC Converter

The output of the Vienna Rectifier will be used as the input for the DC-DC Converter. The goal is to convert a varying DC signal to a steady DC output to power the Wi-Ranger for the sensor package. It was determined in the research section that a synchronous Buck Converter would be the most appropriate option. Based on the Vienna Rectifier output, a proper DC-DC buck converter must be used to produce desirable outputs. The DC-DC converter for this project must take voltages up to 97.97V (peak) and be able to operate with input current of 1.53A. The converter must be able to produce a steady output voltage of 5V and an output current of 3A. After researching various DC-DC Buck Converters that fit above characteristics, the LM5116WG by microchip was found to be the most appropriate. The features for this component are shown in Table 3.2.

Parameters	**Values**
Input Voltage Range	6V to 100V
Output Voltage Range	1.215V to 80V
Peak Gate Current	3.5A
I_Q	<10µA
Operating Frequency	50KHz to 1MHz
Max. Synchronous Operation Frequency	1MHz
VCC, VCCX, ULVO	-0.3V to 16V
HB	-0.3V to 16V
HO	-0.3V to HB+0.3V
LO	-0.3 to VCC+0.3V

Storage Temperature Range	-55°C to +150°C

Table 3.2 - Parameters of the LM5116WG Buck Converter

As seen in the specifications table, the LM5116WG Buck Converter operates at voltage up to 100V which is higher than the desirable 97.97V. Figure 3.8 shows a block diagram of the LM5116WG Buck Converter. The different applications of this converter could be derived by understanding the block diagram.

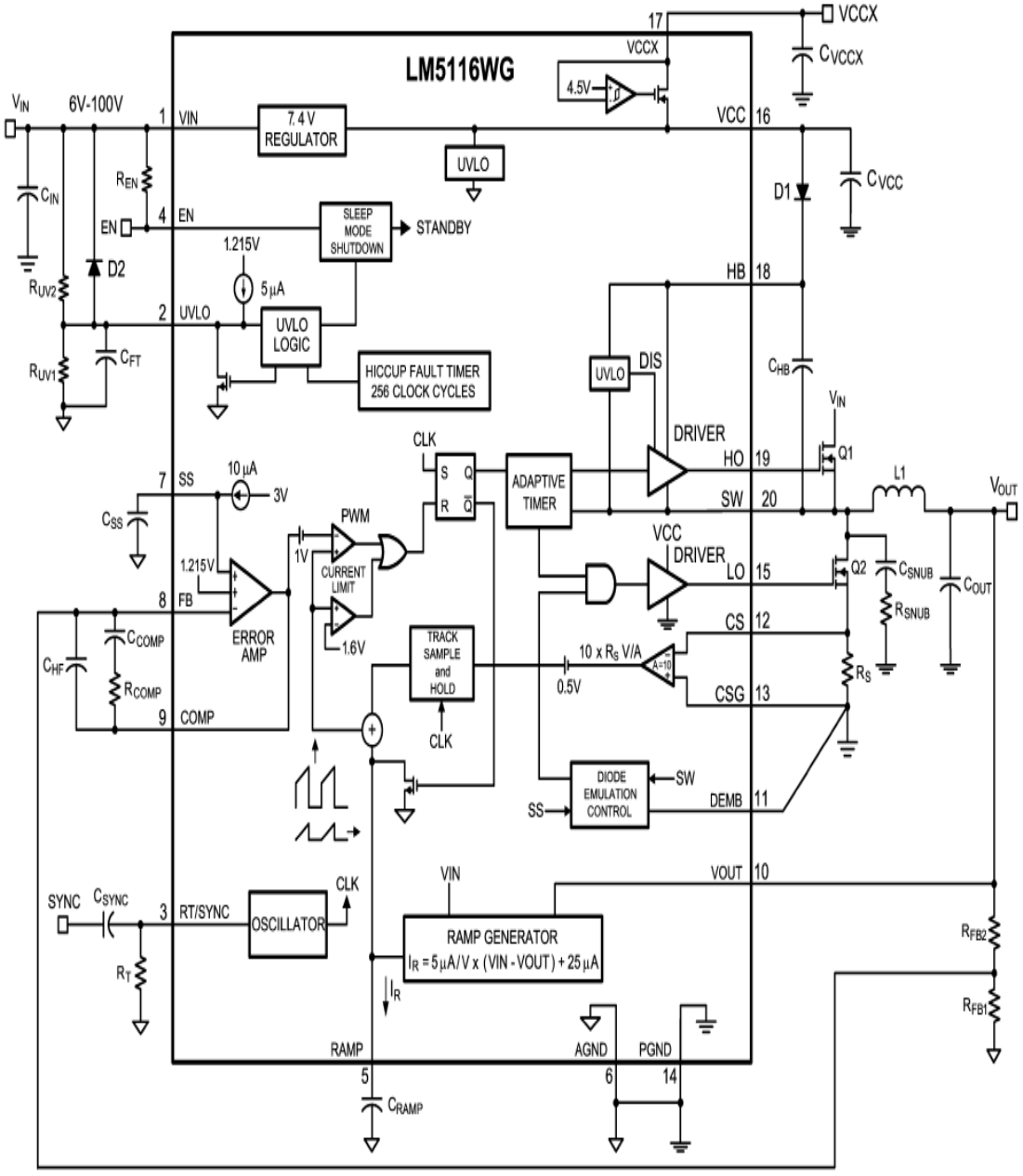


Figure 3.8 - Block Diagram of the LM5116WG Converter (Permissions Requested from National Semiconductor Corporation)

High Voltage Start-Up Regulator – is one of the features embedded inside this converter. This internal dual mode 7.4V regulator also supplies the bias VCC necessary to power the PWM controller.

Oscillator – LM5116WG comes with an inbuilt oscillator that can be easily programmed for maximum frequency oscillation. The equation for which is given below:

$$R_T = \frac{T - 450ns}{284pF}$$

where R_T is the timing resistor in ohms, 450ns is the fixed minimum off time and T = 1/f where f represents the oscillation frequency.

Synchronization Capability – This capability is used to sync the oscillator to an external cycle. It can be achieved by implementing a coupling capacitor parallel to the timing resistor (R_T) with a 5V amplitude signal. This configuration is attached to the RT/SYNC pin (Pin 3). In order to initiate, the nominal amplitude at the pin (1.215V) must be raised above 4V. For normal behaviors of the PWM signal, the synchronizing frequency must not be raised above twice the free-running frequency which is set 15% below the external clock frequency. The coupling capacitor used for such configuration is usually about 100µF.

Under Voltage Lock Out (UVLO) – With the varying nature of the waves, it is possible for the turbines to generate extremely low voltages. LM5116WG features the UVLO pin that puts the converter in stand-by mode if the voltage were to drop below 1.25V. As soon as the voltage gets up to 1.25V and above, the converter starts running in normal mode.

Error Compensation Loop — An error compensation loop is an integral part of this converter. The Error amplifier checks the difference between the regulated output voltage and the 1.25V reference voltage. The output of this amplifier is connected to the pin of the component in order to provide the user an option to connect an external loop compensation network.

Ramp Generator — The ramp generator in the LM5116WG is designed uniquely. Instead of creating large voltage spikes to measure the switch current in generic ramp generators, this generator presents the feature of reconstructing signals. This feature is achieved by using the sample-and-hold DC level and emulated current ramp as shown in Figure 3.9.

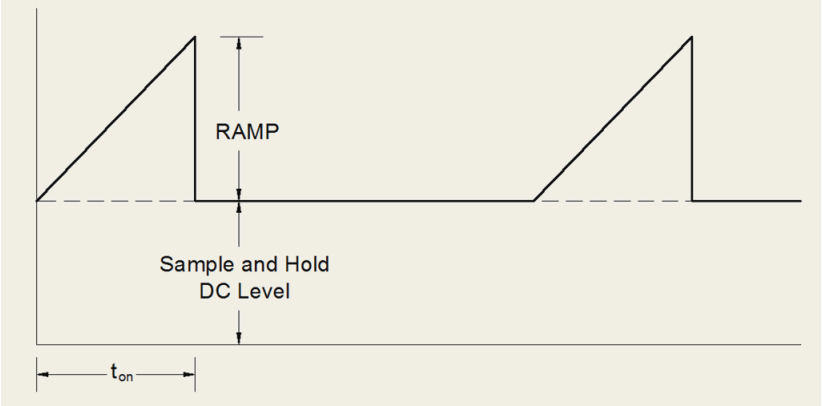


Figure 3.9 - Sample and Hold DC Level and Emulated Current Ramp

The Ramp current could be calculated using the formula:

$$I_R = \left(\frac{5\mu A}{V} \times (V_{in} - V_{out}) + 25\mu A\right) \times \frac{t_{on}}{C_{RAMP}}$$

where C_{RAMP} is the Ramp Capacitor, R_S is the current sense resistor, L is the output inductor and t_{on} is the on time of the generator. Furthermore, the C_{RAMP} value could be calculated as:

$$C_{RAMP} = \frac{g_m \times L}{A \times R_S}$$

where g_m = ramp generator transconductance (5µA/V) and A = current sense amplifier gain (10).

Enable — This is an optional feature of the LM5116WG. This feature shuts down the regulator in case the enable pin (Pin 4) falls below 0.5V. The only way to restore that would be by raising the EN input to 3.3V or above. Figure 3.10 depicts the enable circuit featured in LM5116WG.

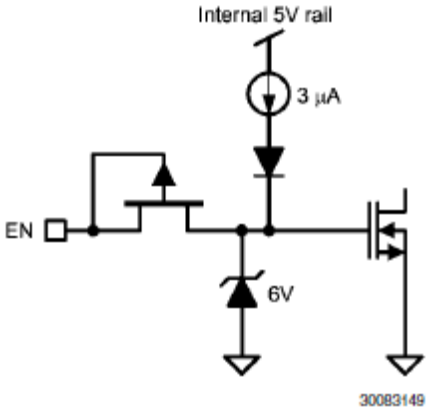


Figure 3.10 - Enable Circuit
(Permission requested from National Semiconductor Corporation)

In case this circuit is not needed in the design, the EN will be attached to the V_{in} with a 1MΩ pull-up resistor, since it cannot be left floating.

Current Limit Monitoring — This is a protection feature implemented inside the converter. This scheme ensures that during overflow of current, the system goes to standby mode. This is done using counter clock cycle. When excess current is detected, the regulator enters the low power dissipation hiccup fault mode and counts the clock cycle using its counter. Once 256 clock cycles are detected, the UVLO is pulled low, shutting down the regulator for an instant. Once the voltage gets back up to 1.215V, the regulator turns back on. The process runs in a loop until the fault is corrected. The current limit and ramp circuit is shown in Figure 3.11.

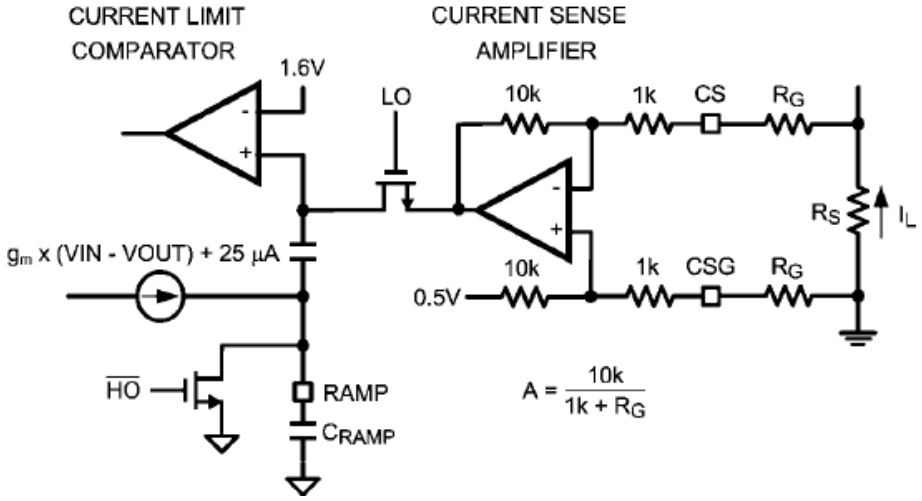


Figure 3.11 - Current Limit and Ramp Circuit
(Permission requested from National Semiconductor Corporation)

The peak current (I_{peak}) can be calculated using the following equation:

$$I_{peak} = \frac{\left(V_{reference} - V_{offset}\right) - \frac{25\mu A \times t_{on}}{C_{ramp}}}{A \times R_S}$$

where $V_{reference}$ is the reference voltage at the current limit comparator and V_{offset} is the offset voltage at the current sensing amplifier.

Soft Start and Diode Emulation — Soft start and diode emulation is another feature offered by the LM5116WG. This feature reduces the initial stress of the converter by gradually progressing toward steady state.

HO & LO Output — The HO pin (Pin 19) delivers a signal to the high end switch while the LO pin (Pin 15) sends a signal to the low end switch of the external components of the converter. HO and LO deliver switching feature to the

converter. When the HO is enabled, LO is disabled. Once the voltage of LO drops to 25% of VCC, HO is enabled after a small delay. Similarly, LO is put to wait as the SW voltage falls up to 50% of VCC. After a small delay, LO enables.

In order to build a design of the buck converter, the values of the external components must be calculated. The final circuit needs to demonstrate the following specifications:

- Output Voltage (V_o) = 5V
- Input Voltage (V_{in}) = 7V to 100V
- Maximum load current (I_o) = 3A
- Switching frequency (f_{SW}) = 300KHz

The values of necessary components will be calculated using simplified equation. The first value that needs to be calculated is that of the timing resistor (R_T). This sets the oscillator switching frequency.

$$R_T = \frac{T - 450ns}{284pF} = \frac{\frac{1}{300KHz} - 450ns}{284pF} = 10.15K\Omega$$

Next is the output inductor. Allowing maximum of 40% ripple current (I_{PP}), the inductor value (L) could be calculated as:

$$L = \frac{V_o}{I_{PP} \times f_{SW}} \times \left(1 - \frac{V_o}{V_{in(max)}}\right) = \frac{5V}{0.4 \times 3A \times 300KHz} \times \left(1 - \frac{5V}{100V}\right) = 13.19\mu H$$

It is known that the maximum current sense signal is produced at minimum voltage. Hence, the resistor value of R_S is calculated. Here, the cycle-by-cycle sense voltage threshold $V_{CS(TH)}$ equals 0.11V as VCCX is assumed to be grounded.

$$R_S \leq \frac{V_{CS(TH)}}{I_O + \frac{V_O}{2 \times L \times f_{SW}} \times \left(1 + \frac{V_O}{V_{in(min)}}\right)} = \frac{0.11}{3 + \frac{5}{2 \times 13.19\mu H \times 300KHz} \times \left(1 + \frac{5}{7}\right)}$$
$$\leq 0.02694\Omega$$

The ramp capacitor is calculated next with the transconductance (g_m) = 5µA/V and the current sense amplifier gain (A) = 10. The values of L and R_S are already known.

$$C_{RAMP} = \frac{g_m \times L}{A \times R_S} = \frac{5\mu A/V \times 13.19\mu H}{10 \times 0.02694} = 244.8pF$$

The output voltage divider level is set by resistors R_{FB1} and R_{FB2}. The ratio of the two is:

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_O}{1.215V} - 1$$

A typical value for R_{FB1} = 1.21KΩ for divider current = 1mA. Therefore, R_{FB2} = 3.74KΩ

The UVLO resistors are placed only if the under-voltage protection is required. In such a case, the values can be calculated as:

$$R_{UV1} = 1.25 \times \left(\frac{R_{UV2}}{V_{IN(MIN)} + (5\mu A \times R_{UV2}) - 1.215} \right)$$

For the design purposes, RUV2 was chosen to be 102KΩ which ensures the shut-down voltage to be 6.6V. Thus the value of RUV1 could be calculated to 21KΩ. Another optional feature provided by the LM5116WG is the current limit or short circuit protection feature. If this feature needs to be utilized, a capacitor CFT of value ≥1μF may be installed in conjunction with a diode D2.

The error amplifier compensation is achieved by configuring R_{COMP}, C_{COMP} and C_{HF}. Precise values must be chosen for these components to achieve fairly accurate error compensation process. There are three main steps in order to determine these values:
The Modulator gain and phase graph (Figure 3.12) relates the required gain of the converter (10) to the desired corner frequency for 5V output. The modulator DC gain of the buck converter could be calculated using the following equation:

$$DC\ Gain\ (modulator) = \frac{R_L}{A \times R_S}$$

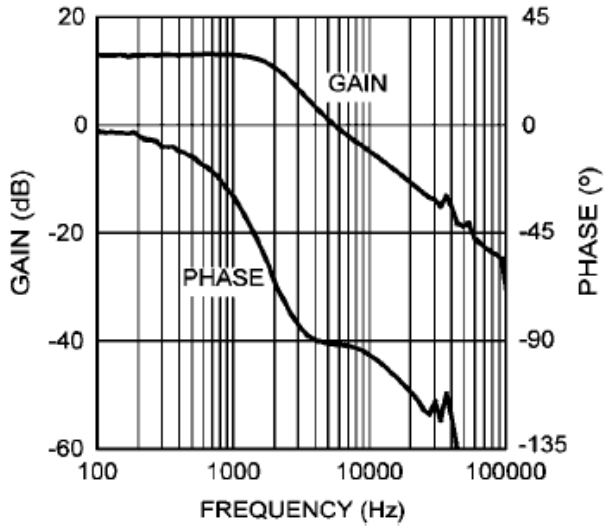


Figure 3.12 - LM5116WG Modular Gain and Phase
(Permissions Requested from National Semiconductor Corporation)

The value of $R_L = \frac{V_O}{I_O} = \frac{5}{3} = 1.667\Omega$. An arbitrary value of the output effective capacitance was chosen as 135µF. Therefore, the modulator corner frequency (f_{mod}) can be calculated as:

$$f_{mod} = \frac{1}{2\pi \times R_L \times C_{eff}} = \frac{1}{2\pi \times 1.667\Omega \times 135\mu F} = 707.2Hz$$

Using these specs, the DC modulator gain is calculated as: $\frac{1.667\Omega}{10\times 0.027\Omega} = 6.17 = 15.8dB$ (as seen in the graph)

Next, the error amplifier gain and phase graph (Figure 13) helped determine the necessary R_{COMP} and C_{COMP} values. This graph shows the error amplifier gain at certain frequencies. This gain is needed to determine the necessary parameters.

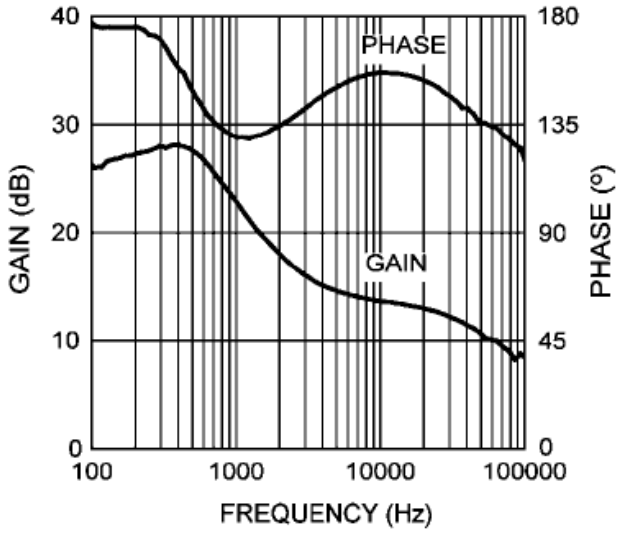


Figure 3.13 - Error Amplifier Gain and Phase
(Permissions Requested from National Semiconductor Corporation)

In order to calculate the R_{COMP} and C_{COMP} values with high precision, the crossover frequency must be chosen. For this design, the crossover frequency was chosen to be 10% of the switching frequency which is 30KHz. Hence, the network compensation frequency or the zero pole frequency (f_z) for R_{COMP} and C_{COMP} is 3KHz. Looking at the graph above, the error amplifier gain can be determined to be approximately 16dB. The equation to calculate R_{COMP} and C_{COMP} is given below:

$$f_z = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} = 3KHz$$

In order to maintain low error amplifier gain, a low resistor value with a relatively higher capacitor value must be chosen. For R_{COMP} = 18 KΩ, the value of C_{COMP} can be calculated as:

$$C_{COMP} = \frac{1}{2\pi \times 18K\Omega \times 3KHz} = 2.947nF$$

For the error amp gain above f_z, the gain could be calculated as $\frac{R_{COMP}}{R_{FB2}} = \frac{18K\Omega}{3.74K\Omega} \approx 13.6dB$

Then, the value of C_{HF} is calculated using the Overall Voltage Loop Gain and Phase graph which is represented in the Figure 3.14. Capacitor (C_{HF}) is necessary in order to reduce the noise in the system. The graph represents the sum of both the gains: Modulator Gain and Error Amplifier Gain.

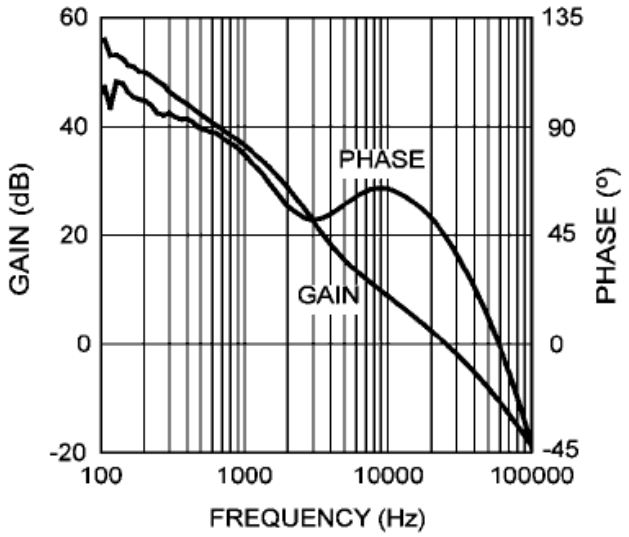


Figure 3.14 - Overall Voltage Loop Gain and Phase
(Permissions Requested from National Semiconductor Corporation)

Using a network analyzer, the overall voltage loop gain can be measured. For the design, the C_{HF} value is arbitrarily chosen as 100pF.

The R_{SNUB} and C_{SNUB} resistor-capacitor network is used to substantially decrease the ringing and spikes. Depending on the system stability, these values could be chosen. The idea is to start at low values of resistor and capacitor since higher values could cause damping and losses.

Finally, to preserve the ideal conditions, certain values were pre-chosen for the following ceramic capacitors:

- 100µF Output Capacitor (C_{out})
- 2.2µF Input Capacitor (C_{in})
- 1µF V_{CC} and V_{CCX} Capacitor (C_{VCC} and C_{VCCX} respectively)
- ≥0.1µF Bootstrap Capacitor (C_{HB})
- 0.01µF Soft-Start Capacitor (C_{SS})

Using the above calculated and estimated values, a basic DC-DC buck converter using the LM5116WG was made using MultiSim. The circuit is represented in Figure 3.15.

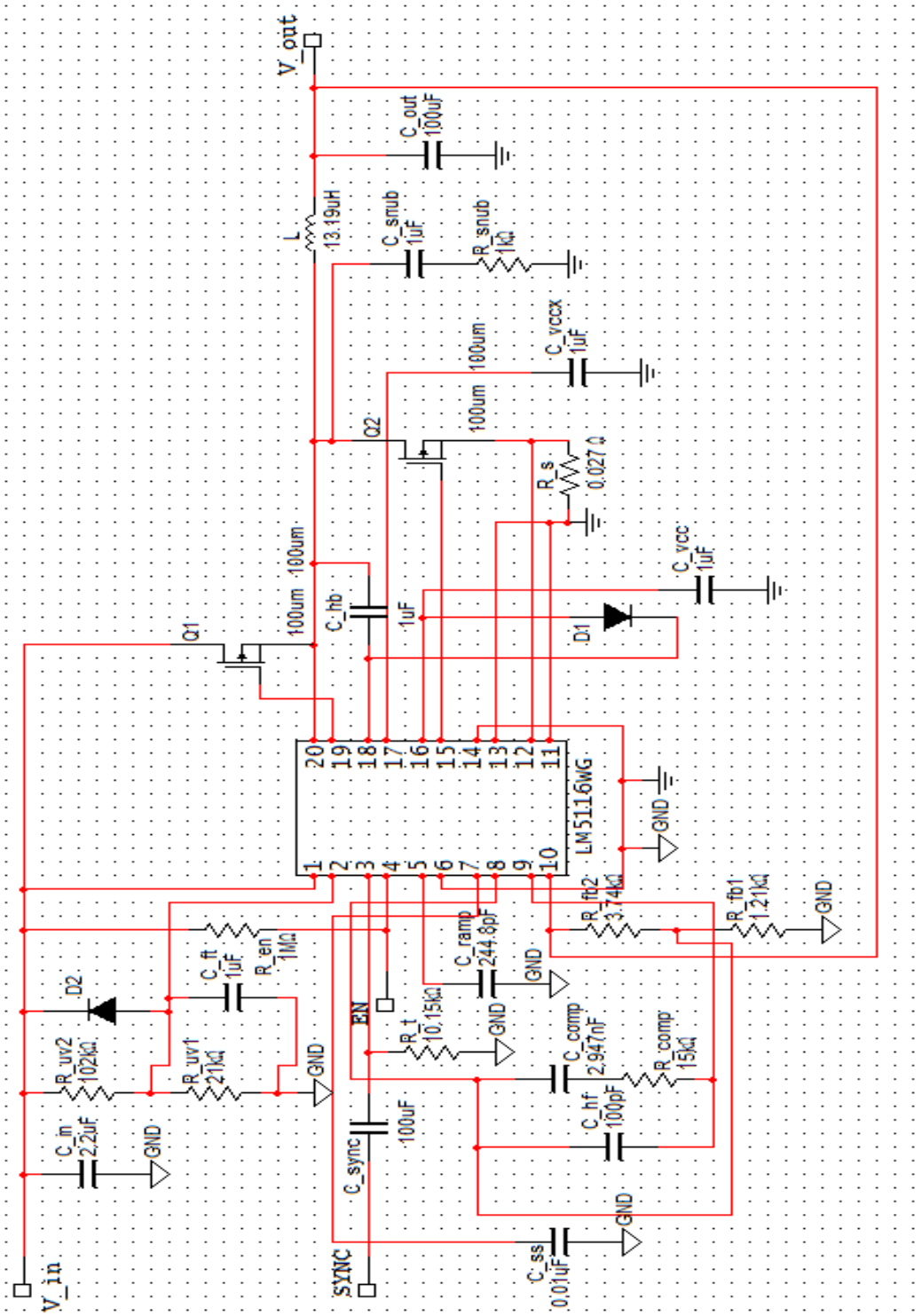


Figure 3.15 - Complete Buck Converter circuit with calculated component values

3.1.3 Charging Circuit Design

Today, there are lots of high end batteries that require efficient solutions for charging circuits that supply long battery life along with high performance. Hence, there is a need to look at different options for such circuits that can provide innovative ideas to achieve high efficiency along with ideal charging conditions. A proper system needs to be initialized for the project that could meet or exceed the necessary requirements. After looking closely at the process of designing a charging circuit, the main conflict was to choose between a custom built microprocessor circuit and an off-the-shelf Integrated Circuit (IC). The difference between the two is reviewed below:

An off-the-shelf IC can be easily acquired for low-voltage charging. However, due to unregulated output, it also is responsible for higher accuracy losses during charging period. A custom built microprocessor circuit could be configured to attain voltage regulation at the output which easily eliminates the losses toward charging accuracy. Another advantage of using a custom built circuit is the advantage of adjusting variations of performance levels. This provides the user with larger efficiency results. Although this feature could be available for an off-the-shelf IC, it is also very likely for its price to be significantly higher. The authentication or communication process between the microprocessor and the host system is likely to be much smoother than that between the off-the-shelf IC and the host system. One of the main differences lies in the ability to perform tasks using simple and easier methods. For example, Figure1 shows the Manual Microprocessor solution to power a four-pack battery with host system communication.

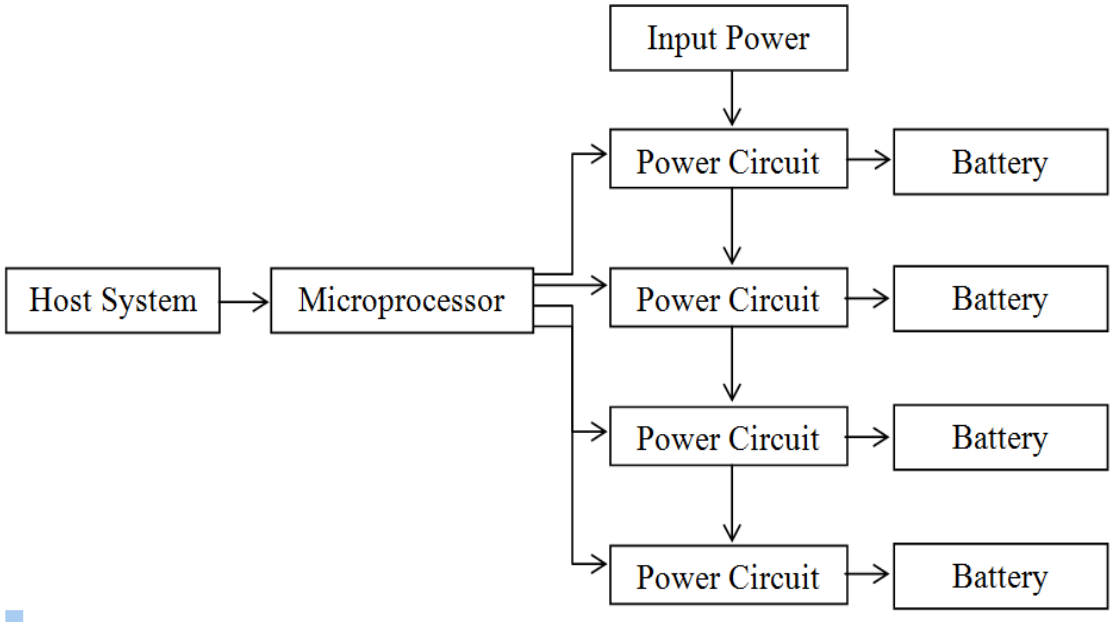


Figure 3.16 - Manual microprocessor solution to power 4-pack battery

Figure 2 show the off-the-shelf IC solution to power a multi-pack battery with host system communication.

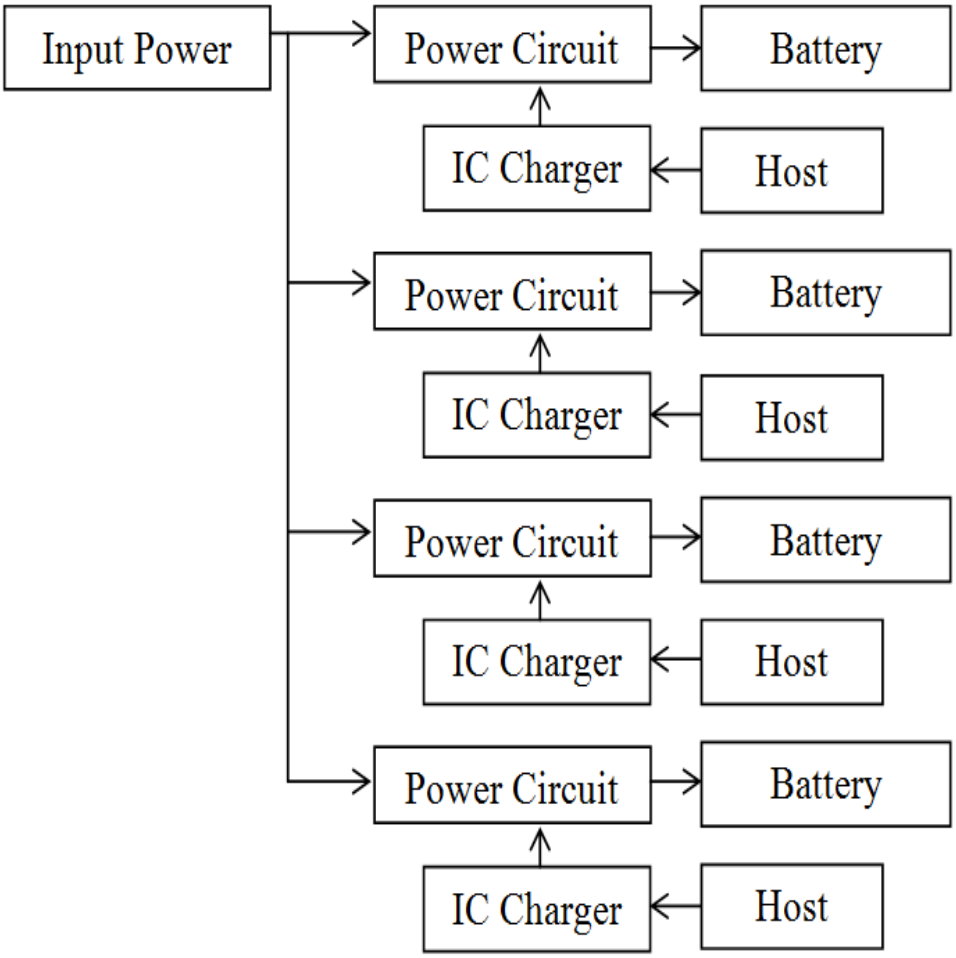


Figure 3.17 - Off-the-shelf IC solution to power 4-pack battery

As seen in Figure 3.16 and Figure 3.17, it can be concluded that using off-the-shelf IC could be way more complex than using a custom microcontroller circuit. Also, the custom microcontroller circuit can considerably reduce the parts of the system. Hence, the custom microcontroller charging circuit was chosen to be the most suitable option.

The design for the power management circuit already uses two dsPIC33f microcontrollers. Thus, it makes sense to implement an intelligent charging circuit that utilizes one of these microcontrollers. This design implements a charger for a lead-acid battery as a sub function in a microcontroller whose main function is several more complicated tasks. The microcontroller receives its power from the same battery. The charging process isn't resource intensive so it doesn't jeopardize the microcontroller's primary tasks. The sub function will be written with three main operating scenarios.

1) the battery is charged
2) the battery is discharged
3) the battery is disconnected

In the first case, the microcontroller must monitor the battery voltage and temperature, as well as control the power switch to maintain optimal battery condition. In the second case, the battery voltage is too low to maintain microcontroller operation. With the microcontroller inactive, the power switch must be on. In the third case, the power switch must also be on. In this condition, the voltage on the microcontroller input is significantly higher than in the other cases. Therefore, the microcontroller input voltage can be used to detect those conditions. The charger's schematic (see Figure 3.18) is broken down into a voltage divider, temperature sensor, MOSFET and MOSFET driver.

The battery voltage through voltage-divider 22k/3.3k goes to the microcontrollers analog to digital input (Volt/AD1). Both the 22k and 3.3k resisters should be temperature stable devices. Battery voltage changes with temperature at about 4 mV/°C/cell. Therefore battery manufacturers recommend incorporating temperature correction in charging circuit designs. Many battery packs already have an integrated temperature sensor. However, not all battery packs come with temperature sensors built in. Furthermore ones that do, often sense the temperature of only one cell.

The optimal solution is to implement a temperature sensor in the circuit itself that sits outside of the battery. This circuit includes a temperature sensor consisting of two diodes and one resistor 4.7k resistor. The diode voltage varies with temperature and is used to double the voltage signal. The sensor's output is connected to the microcontrollers analog to digital input (Volt/AD0). The MOSFET driver circuitry provides voltage gain and level shifting. The driver turns on when the battery is discharged. This starts battery charging. If the battery is disconnected, the microcontroller will detect a very high input voltage and keep the MOSFET on.

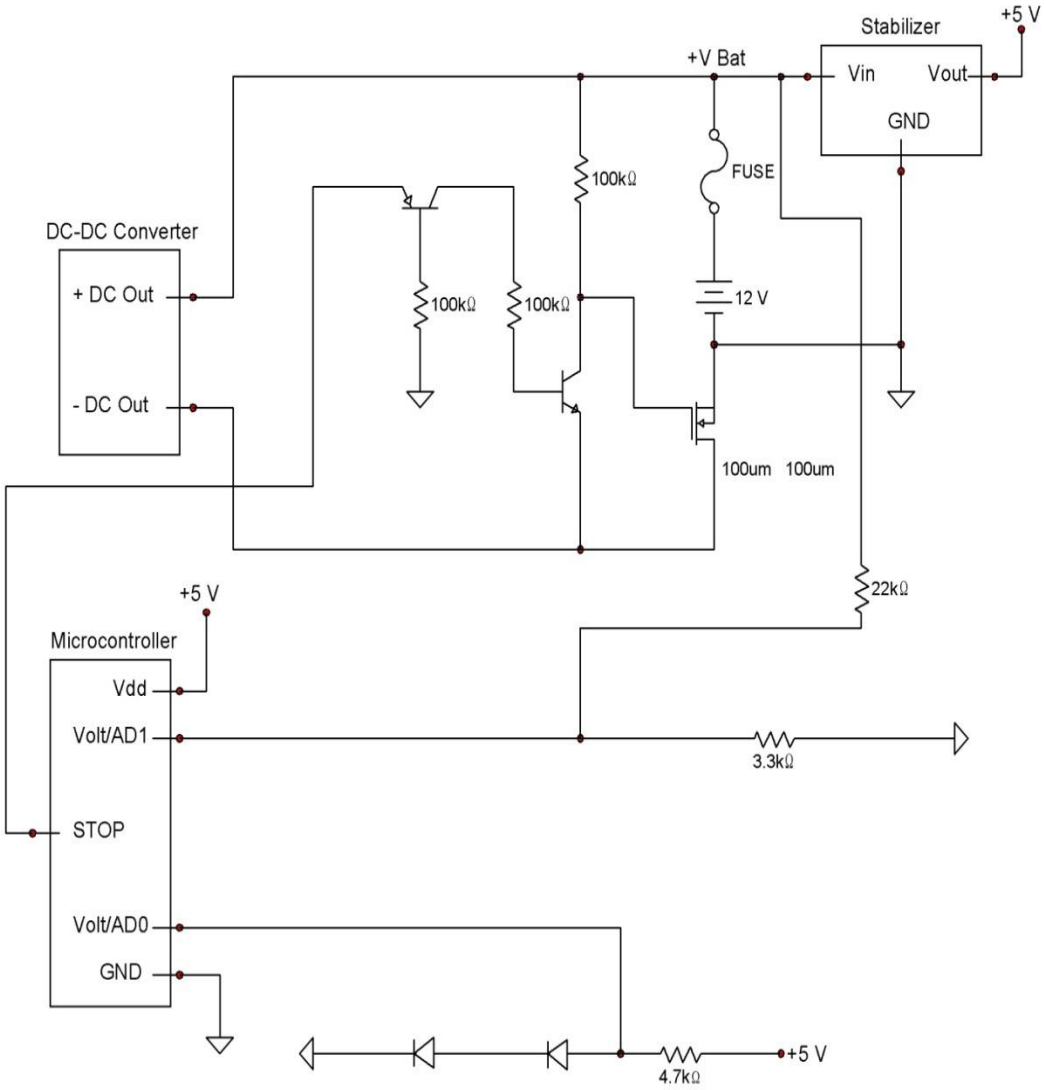


Figure 3.18 - Microcontroller charger circuit schematic

The charging algorithm (shown below) will either charge the battery or maintain battery voltage after it is charged.

```
#define FULL_CHARGE             1           // Full Charging Mode
#define STANDBY_CHARGE      0           // StandBy Charging Mode
#define MosOff()    PORTD |= _BV(4)
#define MosOn()     PORTD &= ~_BV(4)

//AD function
unsigned int AD(unsigned char input){
        unsigned int result;
```

```
        // Reading AD input
        ADMUX=0xC0+input; // Internal REF 2,56V, Right adjusted result
        ADSRA=0XC7; // ADEN, ADSC, -ADATE, -ADIF, -ADIE, ADPS2, ADPS1,
ADPS0
        // Waiting for conversion end
        while(!(ADSRA & _BV(ADIF)));
        // First read ADSL
        result = ADL + (ADH<<8);
        return(result);
}

//Charging algorithm
void ChargerSubfunction(void){
        int V, T; // Input device voltage,
        static char ChargeMode=FULL_CHARGE;

        //AD of input device voltage
        V=AD(1)*2.5*7.666; // 1LSB=2.5mV, divider (22K+3K3)/3K3= 7.666

        //Temperature correction
        T=(518-AD(0))*0.625; // 518 corresponds to 0°C
                //Two diodes gives 2*2mC/C, 1LSB=2.5mV => 2.5mV/4mV=0.645
        V += T*4*6; // 4mv/C/Cell, battery have six cells

        //Checking of input device voltage
        if(V > 17000)MosOn(); // if V>17000mV MOSFET turns-on
        else {
                if(ChargeMode == FULL_CHARGE){
                        if(V > 15000){
                                MosOff(); // if V>15000mV MOSFET turns-off
                                ChargeMode = STANDBY_CHARGE;
                        }
                        else MosOn();
                }
                else if(ChargeMode == STANDBY_CHARGE){
                        if(V < 13000){
                                MosOn(); // if V<13000mV MOSFET turns-on
                                ChargeMode = FULL_CHARGE;
                        }
                        else if(V < 13800) MosOn();
                        else if(V > 14000) MosOff();
                }
        }
}
```

When the waves cause the generator to rotate, the generator will deliver power to the rectifier. The rectifier will deliver power to the charging circuit. At this point, the algorithm enters full charging mode and starts charging the battery with a voltage around 15 V. After the battery is charged, the algorithm enters standby mode and maintains the battery voltage between a lower limit (13.5 V) and upper limit (13.8V). Figure 3.2 illustrates the charging strategy in more detail.

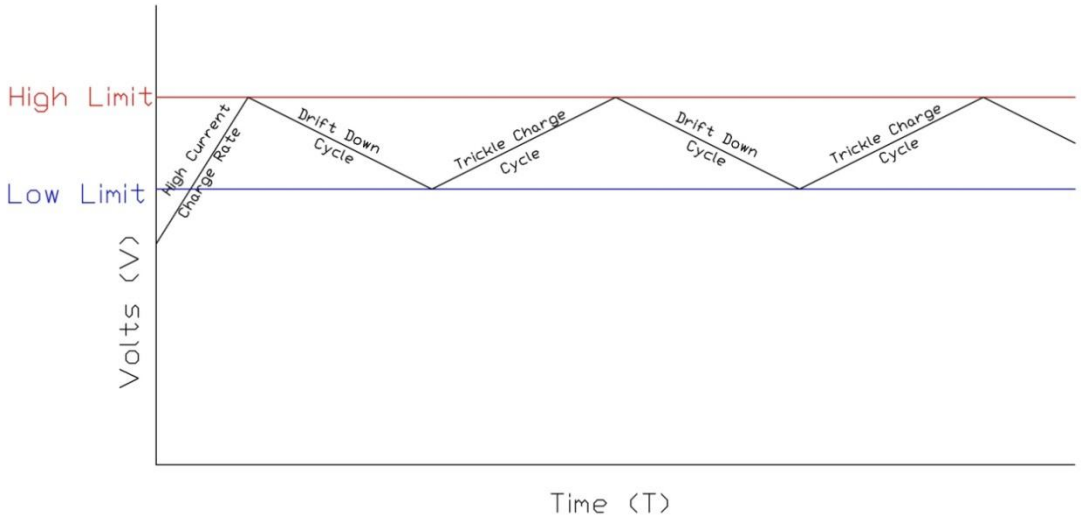


Figure 3.19 - Battery Charging Strategy Utilized in Charging Circuit

The charging circuit and control algorithm will be implemented using a dsPIC33f microcontroller and C compiler.

The circuit will still need to detect charge termination, either using a temperature sensor or using a "negative delta V" cutoff system. The latter is commonly used with NiCd/NiMH packs because their electrical characteristics dictate a sudden drop in voltage right after the battery voltage peaks. However, this charging circuit needs to work with lead acid batteries as well as NiCd/NiMH. So, using a temperature technique is preferred. One such technique could detect a sudden rise in battery temperature to shut off the charge. Other things to consider are the requirement to let a battery cool down, so a better charge can be applied. The charging circuit could wait for the battery voltage to stabilize for about thirty seconds before starting to charge. If the battery has just come off discharge and is hot, it may take a minute or so for the charge to begin to start.

3.1.4 Global Positioning System

The EM-408 GPS module was chosen because it easily interfaces with 3.3V microcontrollers. The actual supply voltage range is from 3.2 V to 3.6 V. The latter is identical to the 16-bit microcontroller chosen. The average current draw of the device is 45mA. This is after the device has acquired satellites. On startup,

the device has an average draw of 75 mA with a peak draw of 90mA. The GPS can also operate in a standby mode that drops the current draw to 0.4 mA. The module can also draw up to 8mA of current to charge a capacitor used for memory storage. This storage feature helps the module to quickly lock onto satellites by storing last location and time information. Additionally, more sensitive external antenna may be added to decrease satellite tracking time and provide the ability to place the antenna away from the electronics. The ground plane characteristics of such an antenna are shown in Figures 3.20 and 3.21.

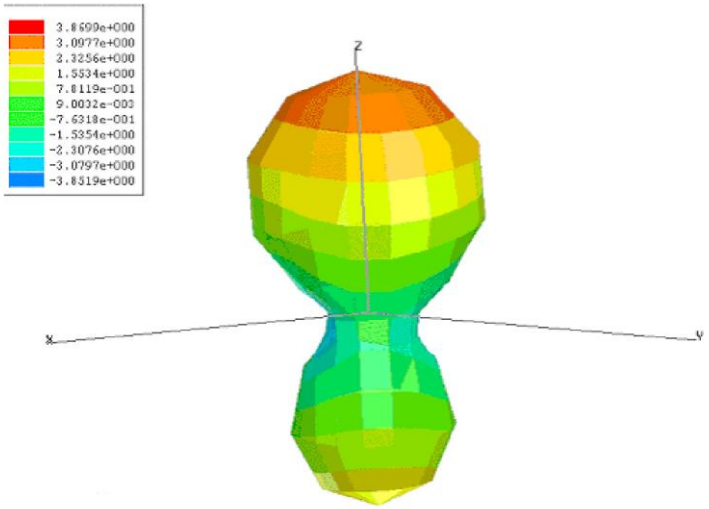


Figure 3.20 - 3-D representations of Antenna Ground Plane Characteristics (Permission requested from Sparkfun)

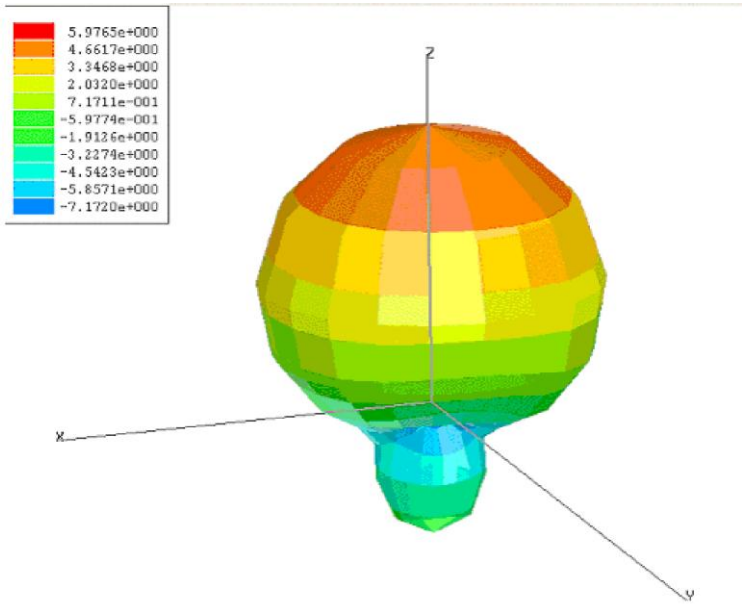


Figure 3.21 - 3-D representations of Antenna Ground Plane Characteristics (Permission requested from Sparkfun)

There are five connections to the module. Two are for power, two are for data and one is used for enable/disable. The enable is active high, so bringing it high will enable the module. Sleep mode is accomplished by bringing it low. If this pin is left floating, it will go low. So, a resistor will be used to pull the pin high. Of the two data connections, one is used for transmit and the other is used for receive. Both of these connections use the standard serial protocol implemented in microcontroller UARTs. So, we can directly connect these pins to the microcontroller. See Figure 3.22.

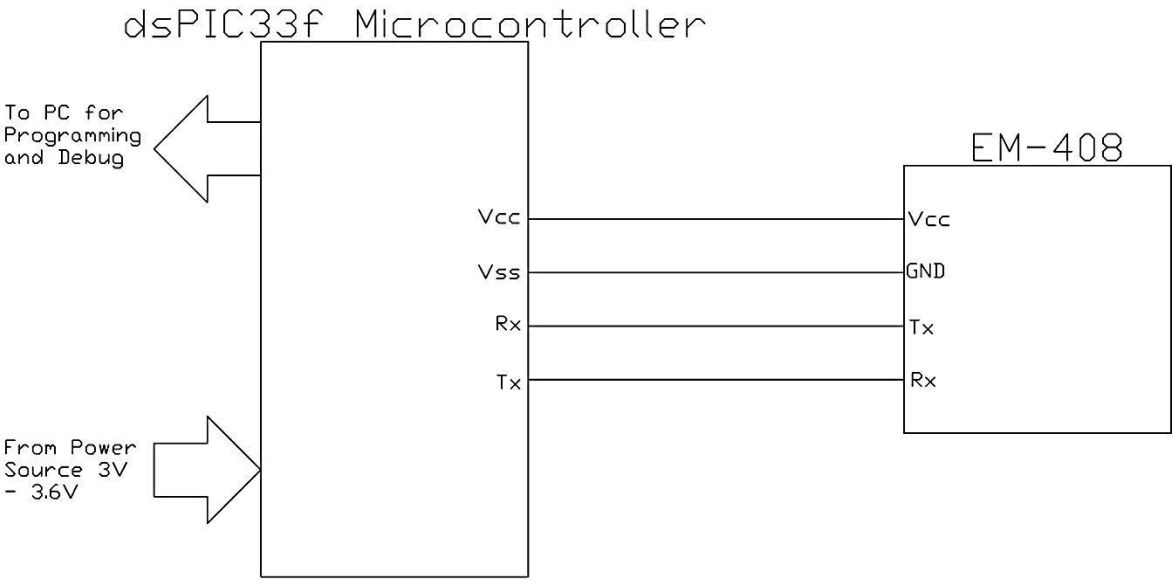


Figure 3.22 - Interfacing EM-408 GPS Module to dsPIC33f Microcontroller

Some documentation stated the receive line must be brought high to work. However, this is false because an internal resistor pulls the line up to the supply voltage. The only issue that might occur is obtaining an error free data stream because of marginal voltage thresholds. Fortunately, our PIC microcontroller has four comparators built in and one can be used to clean up the signal before sending it to the chip's UART. The module transmits data as NEMA messages at 4800 baud with 1 stop bit and no parity. The default NEMA messages outputted are GSA, GSV and RMC. Each line is terminated with a Carriage Return (CR) and Line Feed (LF) pair of characters. The NEMA standard states that the maximum number of characters between the starting $ and the CR/LF pair should be 80 characters. So, the typical output from the module upon startup should resemble the list below.

$PSRFTXT,Version:GSW3.2.4_3.1.00.12-SDK003P1.00a
$PSRFTXT,Version2:F-GPS-03-0701301
$PSRFTXT,WAAS Enable

$PSRFTXT,TOW: 0
$PSRFTXT,WK: 1399
$PSRFTXT,POS: 6378137 0 0
$PSRFTXT,CLK: 96250
$PSRFTXT,CHNL: 12
$PSRFTXT,Baud rate: 4800
$GPGGA,235947.050,,,,,0,00,,,M,0.0,M,,0000*5D
$GPGSA,A,1,,,,,,,,,,,,,,*1E
$GPRMC,235947.050,V,,,,,,,281006,,*29
$GPGGA,235948.057,,,,,0,00,,,M,0.0,M,,0000*55
$GPGSA,A,1,,,,,,,,,,,,,,*1E
$GPRMC,235948.057,V,,,,,,,281006,,*21
$GPGGA,235949.042,,,,,0,00,,,M,0.0,M,,0000*50
$GPGSA,A,1,,,,,,,,,,,,,,*1E
$GPRMC,235949.042,V,,,,,,,281006,,*24
$GPGGA,235950.042,,,,,0,00,,,M,0.0,M,,0000*58
$GPGSA,A,1,,,,,,,,,,,,,,*1E
$GPRMC,235950.042,V,,,,,,,281006,,*2C
$GPGGA,235951.042,,,,,0,00,,,M,0.0,M,,0000*59
$GPGSA,A,1,,,,,,,,,,,,,,*1E
$GPGSV,3,1,12,20,00,000,43,10,00,000,,31,00,000,,27,00,000,*7B
$GPGSV,3,2,12,19,00,000,,07,00,000,,04,00,000,,24,00,000,*76
$GPGSV,3,3,12,16,00,000,,28,00,000,,26,00,000,,29,00,000,*78
$GPRMC,235951.042,V,,,,,,,281006,,*2D
$GPGGA,235952.042,,,,,0,00,,,M,0.0,M,,0000*5A
$GPGSA,A,1,,,,,,,,,,,,,,*1E
$GPRMC,235952.042,V,,,,,,,281006,,*2E
$GPGGA,235953.042,,,,,0,00,,,M,0.0,M,,0000*5B
$GPGSA,A,1,,,,,,,,,,,,,,*1E
$GPRMC,235953.042,V,,,,,,,281006,,*2F
$GPGGA,235954.042,,,,,0,00,,,M,0.0,M,,0000*5C
$GPGSA,A,1,,,,,,,,,,,,,,*1E
$GPRMC,235954.042,V,,,,,,,281006,,*28

After locking onto enough satellites, the module should obtain the correct position and output the data below:

$GPGGA,043356.000,3158.7599,S,11552.8689,E,1,05,3.4,25.0,M,-29.3,M,,0000*56
$GPGSA,A,3,23,20,13,11,32,,,,,,,,4.7,3.4,3.4*31
$GPRMC,043356.000,A,3158.7599,S,11552.8689,E,0.24,54.42,101008,,*20
$GPGGA,043357.000,3158.7598,S,11552.8691,E,1,05,3.4,24.6,M,-29.3,M,,0000*58
$GPGSA,A,3,23,20,13,11,32,,,,,,,,4.7,3.4,3.4*31
$GPRMC,043357.000,A,3158.7598,S,11552.8691,E,0.32,57.59,101008,,*27

$GPGGA,043358.000,3158.7597,S,11552.8692,E,1,05,3.4,24.0,M,-29.3,M,,0000*5D
$GPGSA,A,3,23,20,13,11,32,,,,,,,,4.7,3.4,3.4*31
$GPRMC,043358.000,A,3158.7597,S,11552.8692,E,0.33,58.17,101008,,*20
$GPGGA,043359.000,3158.7597,S,11552.8693,E,1,05,3.4,24.4,M,-29.3,M,,0000*59
$GPGSA,A,3,23,20,13,11,32,,,,,,,,4.7,3.4,3.4*31
$GPGSV,3,1,12,11,75,324,36,01,59,146,27,32,58,161,34,20,56,209,30*75
$GPGSV,3,2,12,23,52,301,40,25,42,101,,13,23,311,23,17,19,237,23*72
$GPGSV,3,3,12,31,12,136,,19,08,358,13,14,06,136,,27,05,350,*72
$GPRMC,043359.000,A,3158.7597,S,11552.8693,E,0.29,58.06,101008,,*2B
$GPGGA,043400.000,3158.7598,S,11552.8693,E,1,05,3.4,25.0,M,-29.3,M,,0000*58
$GPGSA,A,3,23,20,13,11,32,,,,,,,,4.7,3.4,3.4*31
$GPRMC,043400.000,A,3158.7598,S,11552.8693,E,0.20,72.85,101008,,*25

A program will be written on the dsPIC33f Microcontroller to parse the GGA, RMC, GSV, and GSA NMEA commands. The main program will be called parNMEA. This program will call four functions (parGGA, parRMC, parGSV and parGSA) that will parse each of the GGA, RMC, GSV and GSA commands respectively. Each function populates a set of global variables as shown in Table 3.3.

Function	Populated Variable
parGGA	GGA_UTCTime
	GGA_Latitude
	GGA_NS
	GGA_Longitude
	GGA_EW
	GGA_FIX
	GGA_FIXtxt
	GGA_Sats
	GGA_HDOP
	GGA_AltValue
	GGA_AltUnit
	GGA_Sep
	GGA_SepUnits
	GGA_Age
	GGA_Diff
parRMC	RMC_UTC

	RMC_Status
	RMC_Latitude
	RMC_NS
	RMC_Longitude
	RMC_EW
	RMC_SOG
	RMC_COG
	RMC_Date
	RMC_Variation
	RMC_Mode
parGSV	GSV_SATSINVIEW
	GSV_NOM
	GSV_MSG
	GSV_SATIDS(x)
	GSV_SATELE(x)
	GSV_SATAZ(x)
	GSV_SATSNR(x)
parGSA	GSA_SATMODE
	GSA_SATCOUNT

Table 3.3 - GPS Functions and Populated Global Variables

The data from the module was been taken care of. However, it might also be useful to send commands from the microcontroller to the device. One such command is shown below:

$PSRF104,00,00,00,00,00,00,12,08*29

This command resets the module to its factory default configuration. If this command is sent at 4800 baud, it will be received by the device even if the module was placed into the wrong baud rate. The command must be terminated with a CR/LF pair. After being reset to its “factory fresh” state, this module can take at least twelve minutes to determine its location. The latter is because GPS satellites transmit information that enables the module to calculate the satellite’s orbit. After determining the orbit details of enough satellites, the module can calculate its own position. Luckily, this data will be saved in memory. The weather can also affect the satellite acquisition time. The EM-408 is equipped with an MMCX connection that can be used to connect an external antenna. This allows a more sensitive antenna to be used. Also, this antenna can be placed in a better position away from the electronics. The GPS-00464 antenna is a magnet

mount antenna that has a voltage standing wave ratio of less than 2.0. It is powered off 3.3V and has a gain of 26 dB while only drawing 12mA of current. See Figures 3.23 and 3.24.

Figure 3.23 - External Magnet Mount GPS Antenna (Permissions Requested from Sparkfun)

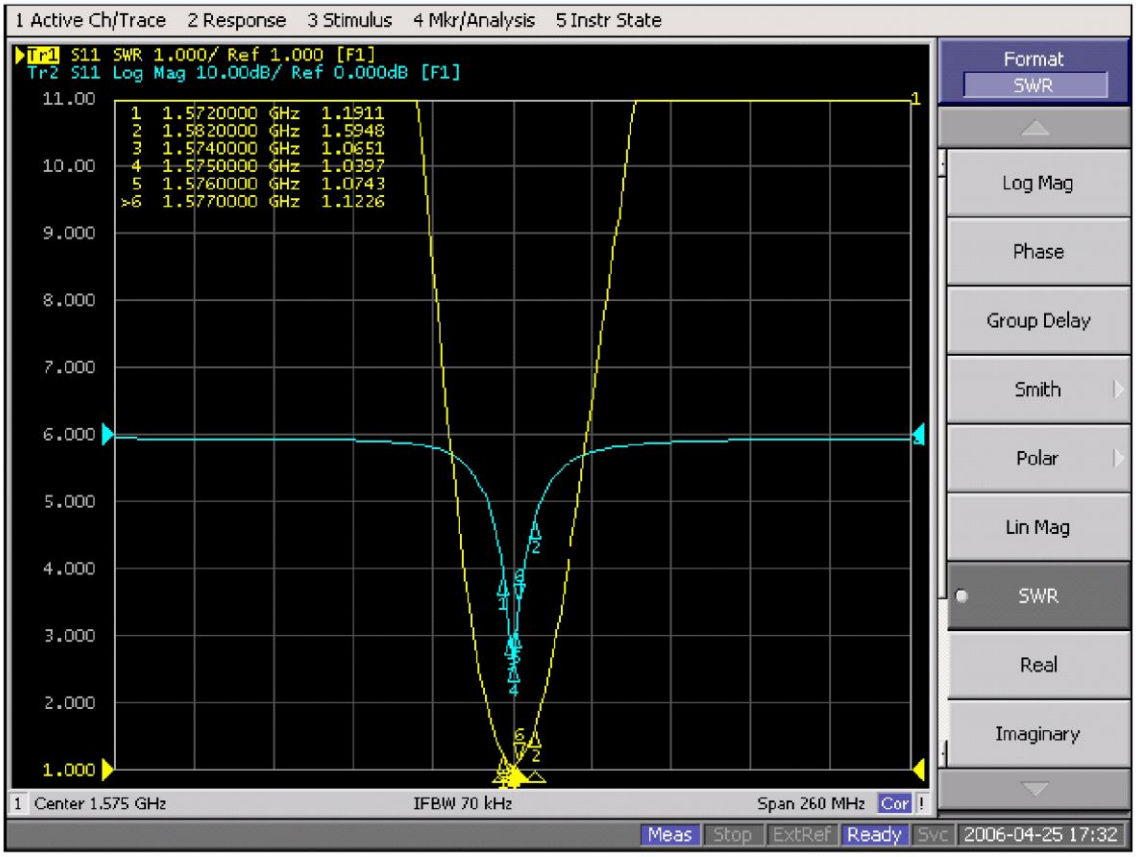


Figure 3.24 - Standing Wave Ratio of External Antenna (Permissions Requested from Sparkfun)

The antenna uses a standard SMA connector. So, an interface cable like the one in Figure 3.25 will need to be purchased.

Figure 3.25 - MMCX to SMA Interface Cable (Permission requested from Sparkfun)

Overall, adding a GPS module to the microcontroller is simple and inexpensive. Having a GPS onboard will help determine that the buoy remains tethered to the rest of the system

3.1.5 System Packaging

Epoxy Potting —The most significant threat to the electrical components of this project in an environment at sea is the constant presence of seawater. Seawater is corrosive, threatening the integrity of any metallic electrical components. It will be necessary to utilize some form of waterproofing in order to protect the project from the waves, rain, and sea spray. In order to accomplish this, it was determined practical to utilize an epoxy potting depicted in Figure 3.26. After the circuitry has been completely assembled, the entire project will need to be coated in an epoxy coating. Further advantages of epoxy potting include electrical isolation and protection from shock and debris.

Figure 3.26 - Two-Part Formula EP 1305 LV Black Epoxy Potting Compound (Permission requested from Ellsworth Adhesives)

Ellsworth Adhesives' Resinlab offers a two-part formula EP 1305 LV Black epoxy potting compound, which would offer excellent protection for the electrical components of this project. Features of the EP 1305 LV Black epoxy that would contribute to the safety of the project include:

- Resistance to water, acids, bases, and most organic solvents
- Shore durometer value of 70 D
- Service temperature of -40° to 150° C
- Volume resistivity of 5.7 x 10^{15} Ω/cm

Enclosure — Because this project is being designed for use at sea, it will need to be adequately protected from a number of physical threats. These include potentially harsh winds, corrosive seawater, marine animal activity, or possibly human manipulation. In order to help ensure the safety of the project, it will not only be treated with an epoxy coating, but it will also be housed in a secure, weatherproof enclosure. This enclosure will need to be comprised of a durable yet non-corroding material if it is to protect the project adequately.

The non-metallic NEMA 4X line of protective enclosures offered by AutomationDirect will provide ideal protection for the project. Figure 3.27 shows a typical non-metallic NEMA 4X enclosure. Features of the NEMA 4X enclosures include:

- Fiberglass construction
- Polyurethane seamless gasket for watertight seal
- Chemical and corrosion resistance
- Rounded edges with minimal protrusions or exposed pocket area for accumulation of debris
- Impact resistance and physical strength greater than that of ABS and PVC

Figure 3.27 - Non-Metallic NEMA 4X Weatherproof Enclosure (Permission Requested from AutomationDirect)

Chapter 4: Testing

4.1 Test Facility

The research testing for this project will primarily take place in the laboratory facilities located on the University of Central Florida main campus in the Engineering I building. The facility offers a variety of resources, including professional assistance, desk space, computer access with features available for simulation, and test equipment, including a hydraulic wave simulator and a Ginlong generator.

4.2 Testing Procedures

Although UCF has developed a platform to simulate deep ocean waves, the mechanical energy team is still working on the turbine design. Therefore, another method of testing the power management circuit will need to be created. Instead of connecting the turbine to the Ginlong generator shaft, an electric motor can be used instead. However, we still need the motor to rotate the generator shaft at different speeds in a random pattern. This can be accomplished by using a speed controller. The speed controller can be loop through a logic circuit that generates random voltage levels within a specified range. A DC motor will be used because DC motors are easier to control than their AC counterparts. The three phase output of the generator will still be connected to the AC-DC rectifier. The torque specifications of the DC motor will need to exceed those required to rotate the shaft of the Ginlong generator. In fact, to simulate strong waves, the DC motor will need to be capable of increasing the generator RPM in a short time span.

Before getting to that stage, the hardware and software will need to be tested individually. Hardware components can be tested with an oscilloscope, multimeter and signal generator. The microcontroller code will be tested with a circuit emulator and debugger to step through faulty code. After getting the microcontroller to function, it can be connected to a PC and efficiency data will be extracted. This data will be verified with an oscilloscope. While the PC and oscilloscope are connected to the circuit, the temperature will be varied to extremes to test the circuit's ability to withstand harsh environmental conditions.

The rectifier output will be verified with an oscilloscope. The output signal will be analyzed over the entire range expected generator RPMs. This will produce an input signal of many frequencies and amplitudes. The generator RPM will be sharply increased and decreased to simulate the sudden rise and fall of ocean waves. Particular attention will be given to ensure the hardware is functioning correctly. This includes verifying that the power factor correction and maximum

power point tracking algorithms are working as expected. PFC can be tested by using a wattmeter and comparing the true power measured across a resistive test load to the apparent power calculated using the voltage and current through the resistive load. Both hardware and software might need to be modified until the percentage of error between the actual and calculated power is satisfactory. Sometimes the error can be due to wide tolerances in the hardware or the speed of the microcontroller. Microcontroller speed affects the control algorithm that handles PFC. If this is an issue, developing a more efficient algorithm will be attempted first before replacing the microcontroller. An algorithm can also be improved by compiling it on a more advanced compiler. One drawback is the price of advanced compliers and the debugging difficulties that arrive when algorithms become altered. Some problems, like the lack of necessary resolution of an analog to digital converter can only be solved by replacing the microcontroller.

The maximum power point tracking algorithm will need to be tested independently of the PFC algorithm. Unchecked errors in the PFC algorithm can inadvertently be passed to the MPPT algorithm. The easiest way to avoid this complication is to fully test and verify the operation of the PFC components and algorithm. Although the ideal power factory is unity, a PF between 0.8 and 1.0 will suffice. Just as important as the PF itself, there is a need for the PF to be stable and not vary suddenly from a particular value. If the PF is stable, then the MPPT algorithm and components can be tested. The power point can be observed by plotting the voltage versus the current of the system. This information can be obtained via the PC interface. Plotting this data will visually depict how well the algorithm tracks the maximum power point. Rather than actually use a battery, constant load impedance will be used instead.

The step down DC to DC converter will be tested by varying its input voltage from 10 V to 100 V and verifying a steady output of 5 V. There are a plethora of parameters to verify a DC to DC converter is operating correctly. Using the formulas below will ensure the DC to DC converter is functioning in a normal manner.

$$\text{Output Voltage Accuracy} = \left[\frac{V_{ON}-V_O}{V_O}\right] * 100\%$$

$$\text{Regulated Line Regulation} = \left[\frac{V_{ON}-V_D}{V_{ON}}\right] * 100\%$$

$$\text{Unregulated Line Regulation} = \left[\frac{\left(\frac{V_{ON}-V_D}{V_{ON}}\right)}{\Delta V_{IN}\%}\right] * 100\%$$

$$\text{Load Regulation} = \left[\frac{V_{OM}-V_{OF}}{V_{OF}}\right] * 100\%$$

$$\text{Efficiency} = \left[\frac{V_{ON}I_{ON}}{V_{IN}V_{IN}}\right] * 100\%$$

The hardest parameter to measure is the output ripple and noise. The ripple will be measured in peak-to-peak millivolts. The output ripple must be measured with a 20 MHz oscilloscope because the output ripple is a series of small pulses with high frequency content. The measurement itself must be made with great care and with special high frequency probes. Even the conventional ground clip can't be used because it will act as an antenna and induce an erroneous voltage that isn't part of the output noise of the converter. Ultimately, the goal is to obtain all the significant harmonics of ripple spikes. If the output ripple is deemed unacceptable, a good quality, low ESR capacitor will be placed as close as possible across the load. Lastly, the transient recovery time and transient response deviation can be measured by rapidly changing the connected load.

The charging circuit will first be tested without a battery connected. Instead an electronic model of a battery will be used. A battery can be modeled as a voltage source with capabilities for both current sourcing (discharge) and current sinking (charge), in series with a resistor representing the battery's internal resistance. Then, the voltage and current of the resistor will be measured to determine the efficiency of the circuit. The output voltage should remain steady if it is going to be used to charge a battery. If the charging circuit performs satisfactorily, the model will be replaced with a lead acid battery. It will be verified that the battery is charged correctly and that the charging algorithm is able to handle potential problems such as overheating, overcharging, short circuit, and the battery being disconnected. Overheating and overcharging can both be tested by connecting a fully charged battery to the circuit and monitoring the current and temperature. The current should be a trickle charge and shouldn't be applied constantly. Rather, it should be applied off and on in long pulses. This method of charging will also prevent overheating. A short circuit test will be performed by disconnected the battery and connecting the positive and negative terminals directly to one another. The controller should immediately stop the flow of current.

4.3 Communication

The power management circuit must have mandatory communication between the microcontrollers and optional communication between the master microcontroller and a PC. Both of these areas will be tested. The master microcontroller must also store information to onboard flash memory for later retrieval. The PC to master microcontroller communication will be fairly simple to test. First, the PC will be tested by supplying packets constructed through a test interface. This ensures that any errors that occur during the test can only be blamed on the PC and not the microcontroller.

The PC test will only be considered a success once all packet types have been sent, received and verified. Then, communication with the master DSP may be

tested. The first test will be a simple loop back scheme. The DSP will be sent packets that it needs to tear down, rebuild and send back to the PC. If the data sent back passes an integrity check, the communication will then be tested along with the control software. The master microcontroller should continually transmit system parameters and observed electrically parameters. These parameters include voltages, currents, and frequencies. Besides transmitting these parameters, the microcontroller should be able to modify the parameters when instructed by an appropriate command.

Testing the slave microcontroller communication will also begin with a simple loop back scheme. The loop back scheme must include tearing the packet down and rebuilding it to ensure that the microcontroller can successfully parse the data coming in. If the microcontrollers can loop back information to each other, then their SPI communication is verified and the test will be repeated with the slave microcontroller's control algorithm running. If everything goes smoothly, the system response will be controlled and monitored from the PC and from the oscilloscope to ensure everything checks out.

Perhaps the easiest communication to test is between the microcontroller and it's onboard flash memory. For this test, the data sent to the onboard flash will also be sent to the connected PC. The data will then be extracted from the onboard flash and compared with the data sent to the PC. If the data is identical, the test was a success and all communication has been verified.

4.4 System Test

The entire system will be tested on a test rig shown in Figure 4.1. The test is very close to a real world simulation. The test rig will be used long enough to observe how the system performs under different environmental factors such as temperature, wind and humidity variations. The system test helps discover flaws in the system that may not appear during the individual stages and software. A slight variation in one parameter such as temperature can easily manifest itself in unexpected areas such as input signals which could in turn affect the software algorithms. In short, testing isn't complete until the whole system has been extensively run through its paces.

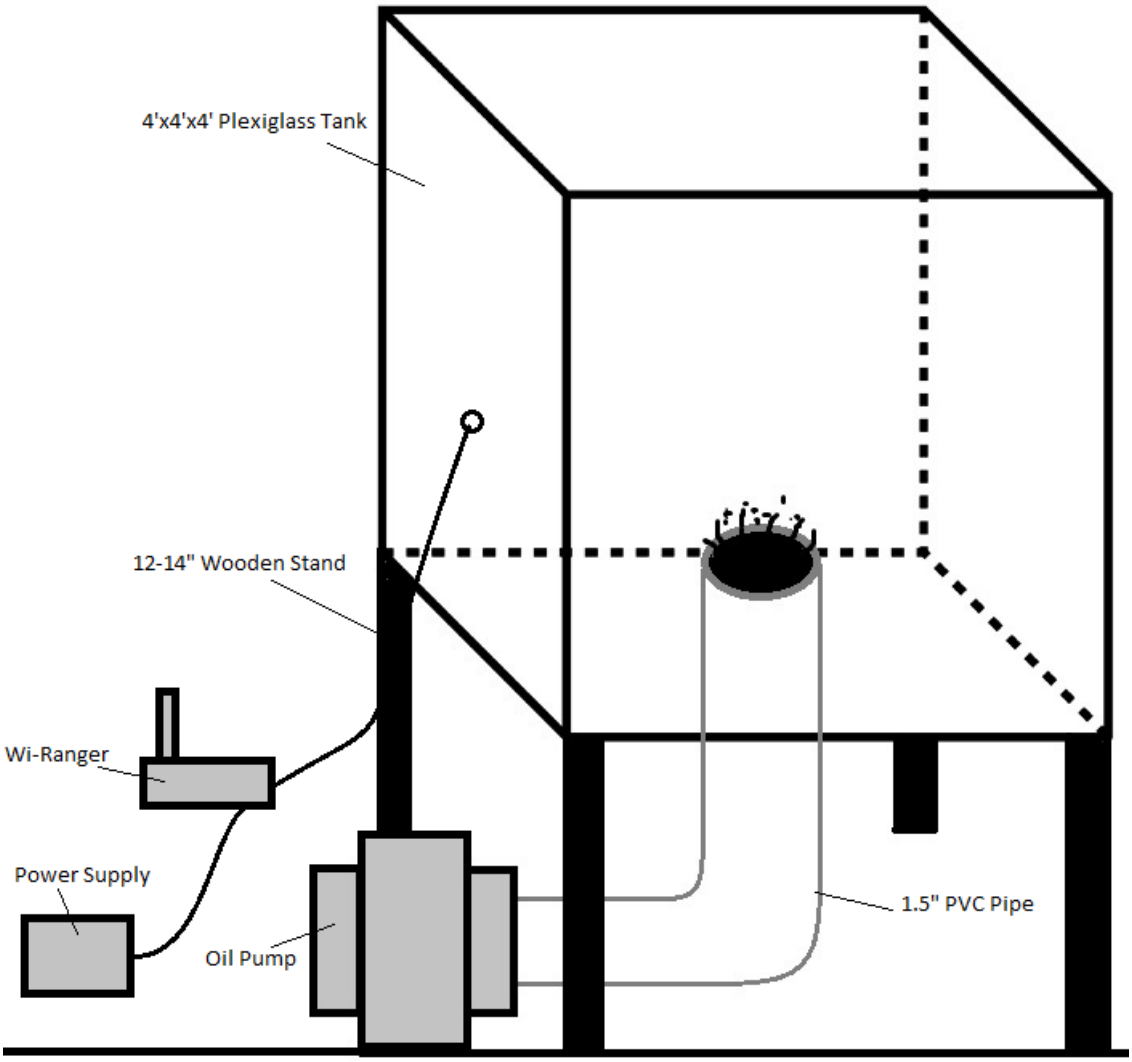


Figure 4.1 - System Test Rig (Provided by Sensor Team)

Chapter 5: Summary

5.1.1 Parts Procurement

The design of various key components such as the Vienna Rectifier and Buck converter were used in order to determine different parts of that needed to be acquired. Also, some equipment will already be available for use from either the research lab or other teams. That also includes the ginlong generator and the wave turbine.

The other parts that will not be readily available will be acquired through the market. Wide varieties of individual components such as resistors, capacitors, op-amps, etc. are available for use. These components are produced by reputable manufactures such as Microchip, National Semiconductor, International Rectifier, etc. Digi-Key is one of the largest distributors for such parts. Most of the parts could be easily obtained from Digi-Key and hence it remains one of the most valuable suppliers for this project.

After research, it was found that lot of the parts required to design the prototype could easily be acquired through sampling from these manufacturers. Fortunately, this process will be able to save money as the sample parts would be free of cost. Also, some manufacturers provide free samples every few months which is an option available on request. Sampling of parts will ensure savings and help reduce the total cost of the project.

For the parts that cannot be sampled, they will be purchased from the supplier; the supplier most likely being Digi-Key. Cheapest options will be considered during the purchase stage. It is highly desirable to acquire all the parts as soon as possible, preferably by January in order to have an early start for the design and development process. An estimated parts list is shown in the Table 5.1:

Parts List					
Component	**Manufacturer/ Distributor**	**Part Number**	**Quantity**	**Unit Price ($)**	**Extrapolated Price ($)**
Turbine			1		
Generator	Ginlong	GL-PMG-500A	1		
Microcontroller, VIENNA	Microchip	dsPIC33FJ16GS504	1	5.34	5.34
Microcontroller, Buck	Microchip	dsPIC33FJ16GS504	1	5.34	5.34
Op Amp	National Semiconductor	LM124AJ	10	4.00	40.00
MOSFET, VIENNA	International Rectifier	IRL2910PBF	30	1.43	42.90
MOSFET, Buck	International Rectifier	IRFP4410ZPBF	8	1.58	12.64

MOSFET, Charging Circuit	Digi-Key	DMB53D0UDWDICT-ND	1	0.44	0.44
DC-DC Converter, Buck	National Semiconductor	LM5116WG	1	7.12	7.12
Capacitor, 100 µF	Digi-Key	490-4512-1-ND	10	1.606	16.06
Capacitor, 2.2 µF	Digi-Key	445-3450-1-ND	10	0.088	0.88
Capacitor, 1 µF	Digi-Key	445-1328-1-ND	10	0.035	0.35
Capacitor, 100 nF	Digi-Key	490-1318-1-ND	10	0.013	0.13
Capacitor, 10 nF	Digi-Key	490-1312-1-ND	10	0.013	0.13
Capacitor, 3 nF	Digi-Key	490-1631-1-ND	10	0.188	1.88
Capacitor, 240 pF	Digi-Key	490-1436-1-ND	10	0.084	0.84
Capacitor, 100 pF	Digi-Key	BC2348-ND	10	0.015	0.15
Resistor, 102 kΩ	Digi-Key	RMCF0402FT102KCT-ND	1	0.04	0.04
Resistor, 100 kΩ	Digi-Key	RMCF1206JT100KCT-ND	3	0.05	0.15
Resistor, 22 kΩ	Digi-Key	RMCF1206JT22K0CT-ND	1	0.05	0.05
Resistor, 21 kΩ	Digi-Key	RMCF0402FT21K0CT-ND	1	0.04	0.04
Resistor, 15 kΩ	Digi-Key	RMCF1206FT15K0CT-ND	1	0.06	0.06
Resistor, 10.15 kΩ	Digi-Key	RMCF1206FT10K2CT-ND	1	0.06	0.06
Resistor, 4.7 kΩ	Digi-Key	RMCF1206JT4K70CT-ND	1	0.05	0.05
Resistor, 3.3 kΩ	Digi-Key	RMCF1206JT3K30CT-ND	1	0.05	0.05
Resistor, 1 kΩ	Digi-Key	RMCF1206FT1K00CT-ND	1	0.06	0.06
Resistor, 27 mΩ	Digi-Key	CSNL1206FT3L00CT-ND	1	$1.05	1.05
Total Cost					135.71

Figure 5.1 - Parts List

5.1.2 Conclusion

This project was geared towards developing a system that could efficiently convert a varying AC signal from the wave turbine generator to a steady 5VDC signal output. The conversion method of this process was presented in this report using various hardware and software components. The entire system was presented using various design elements including multisim simulations, graphs,

tables, etc. Finally, the parts list was compiled and formulated in order to adequately prepare the team for the Senior Design II phase.

Appendix A

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